

36Mb Sync. Pipelined Burst SRAM Specification

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Document Title

1Mx36 & 2Mx18 Bit Synchronous Pipelined Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 2012	Preliminary
1.0	Add Current Value	Jan. 2013	Final
1.1	Add 165FBGA information	Mar. 2013	Final
1.2	Add 1.8V Vdd support	Nov. 2014	Final
1.3	Correct typo in ordering information S7A32xx31M => S7A32xx30M	May 2017	Final

S7A323630M S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

1Mx36 & 2Mx18 Bit Synchronous Pipelined Burst SRAM

Features

- $V_{DD} = 1.8V (1.7V \sim 2.0V)$ or
2.5V (2.3V ~ 2.7V) or
3.3V (3.1V ~ 3.5V) Power Supply
- $V_{DDQ} = 1.7V \sim 2.0V$ I/O Power Supply ($V_{DD}=1.8V$) or
2.3V ~ 2.7V I/O Power Supply ($V_{DD}=2.5V$) or
2.3V ~ 3.5V I/O Power Supply ($V_{DD}=3.3V$)
- Synchronous Operation
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter
- Self-Timed Write Cycle
- On-Chip Address and Control Registers
- Byte Writable Function
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal
- \overline{LBO} Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable
- Asynchronous Output Enable Control
- \overline{ADSP} , \overline{ADSC} , \overline{ADV} Burst Control Pins
- TTL-Level Three-State Output
- Operating in commercial and industrial temperature range
- 100-TQFP-1420A (Lead free package)
- 165FBGA(11x15 ball array) with body size of 13mmx15mm. (Lead free package)

General Description

The S7A323630M and S7A321830M are 32,748,736-bit Synchronous Static Random Access Memory designed for high performance.

It is organized as 1M(2M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance applications; \overline{GW} , \overline{BW} , \overline{LBO} , \overline{ZZ} . Write cycles are internally self-timed and synchronous.

Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with \overline{CS}_1 high, \overline{ADSP} is blocked to control signals.

Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

\overline{LBO} pin is DC operated and determines burst sequence(linear or interleaved).

\overline{ZZ} pin controls Power Down State and reduces Stand-by current regardless of CLK.

The S7A323630M and S7A321830M are fabricated using high performance CMOS technology and is available in a 100pin TQFP package and 165FBGA package. Multiple power and ground pins are utilized to minimize ground bounce.

Key Parameters

Parameter	Symbol	-25	-16	Unit
Cycle Time	tCYC	4.0	6.0	ns
Clock Access Time	tCD	2.6	3.5	ns
Output Enable Access Time	tOE	2.6	3.5	ns
Operating Current	I _{cc}	300	260	mA
Standby Current	I _{SB2}	120	120	mA

36Mb Synchronous Pipelined Burst SRAM Ordering Information

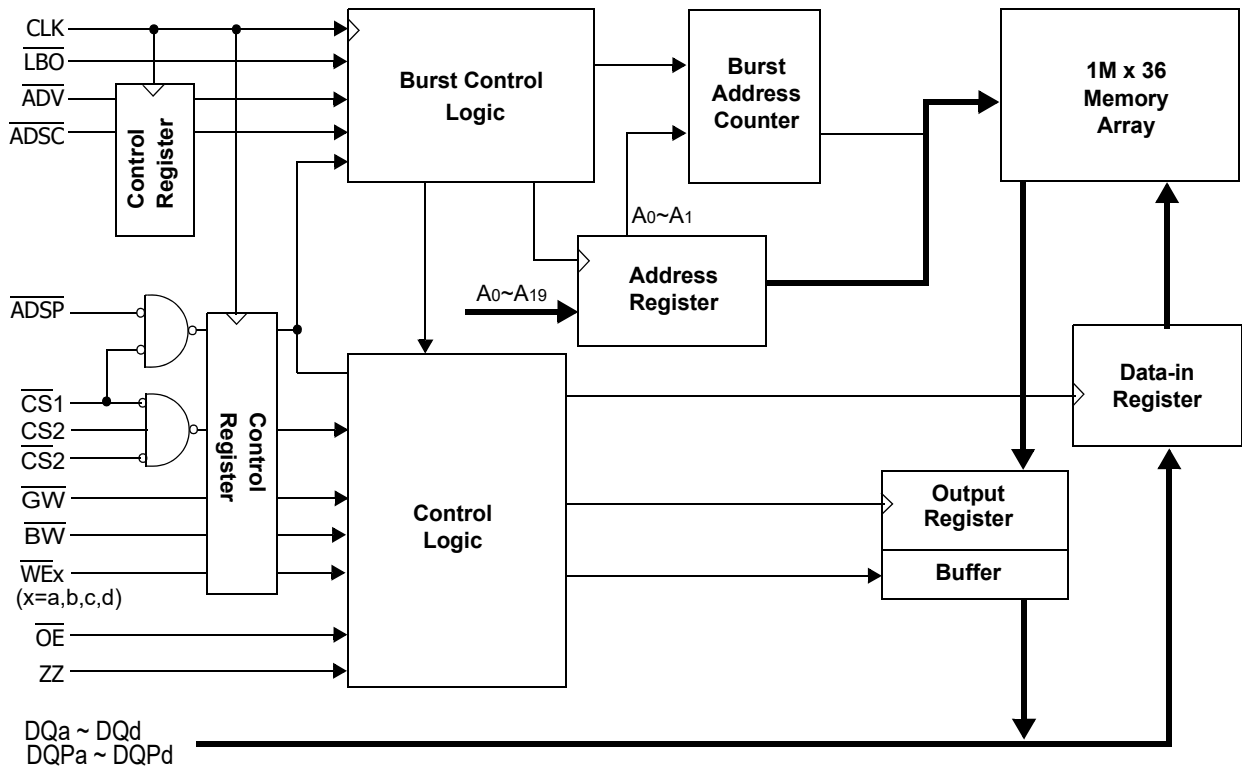
Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
2Mx18	1.8	4.0	3.0	S7A321830M-P(E)C(I)25	0
	3.3/2.5	4.0	2.6	S7A321830M-P(E)C(I)25	0
	3.3/2.5/1.8	6.0	3.5	S7A321830M-P(E)C(I)16	0
1Mx36	1.8	4.0	3.0	S7A323630M-P(E)C(I)25	0
	3.3/2.5	4.0	2.6	S7A323630M-P(E)C(I)25	0
	3.3/2.5/1.8	6.0	3.5	S7A323630M-P(E)C(I)16	0

Note 1. P(E) [Package type] : P - 100TQFP Pb Free, E - 165FBGA Pb Free
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

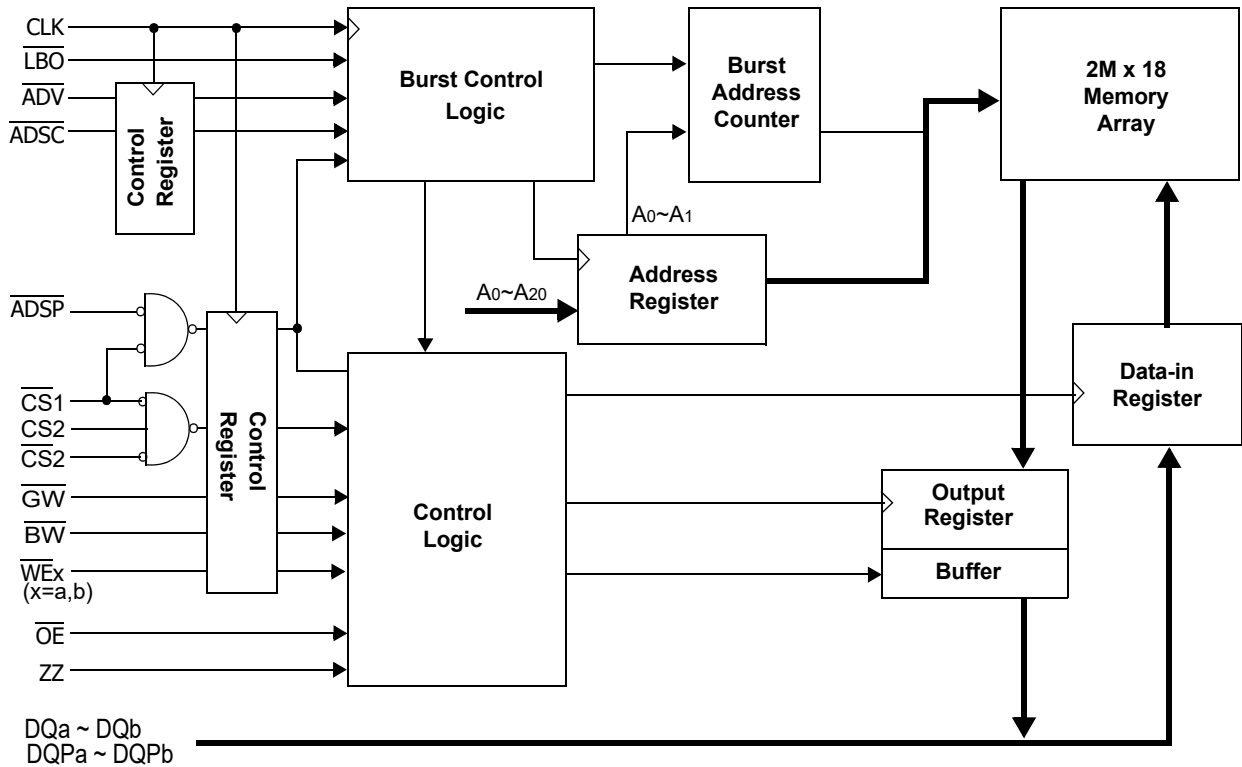
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Logic Block Diagram - S7A323630M (1M x 36)



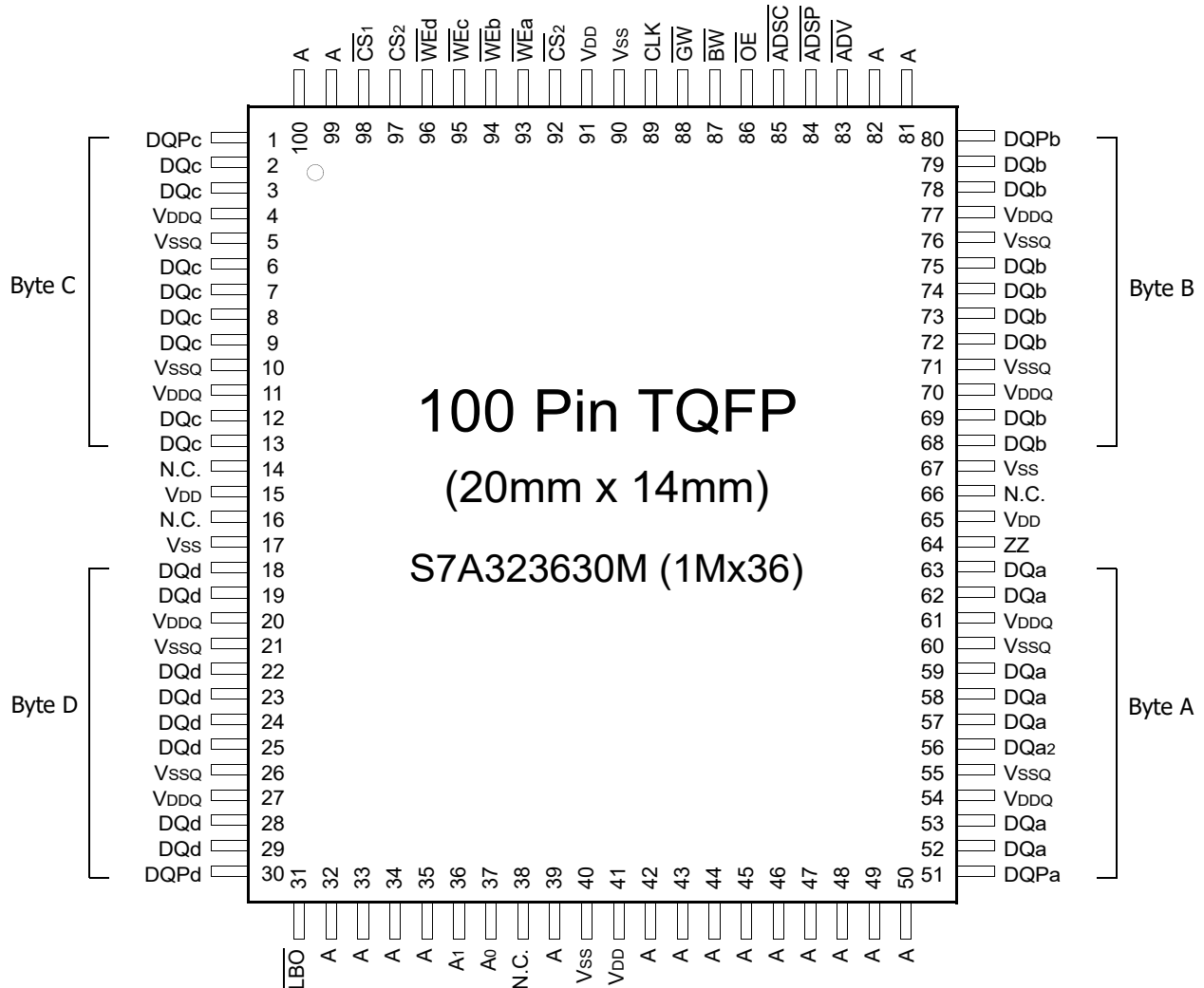
Logic Block Diagram - S7A321830M (2M x 18)



S7A323630M S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

100 TQFP Package Pin Configurations(Top View)



Pin Name

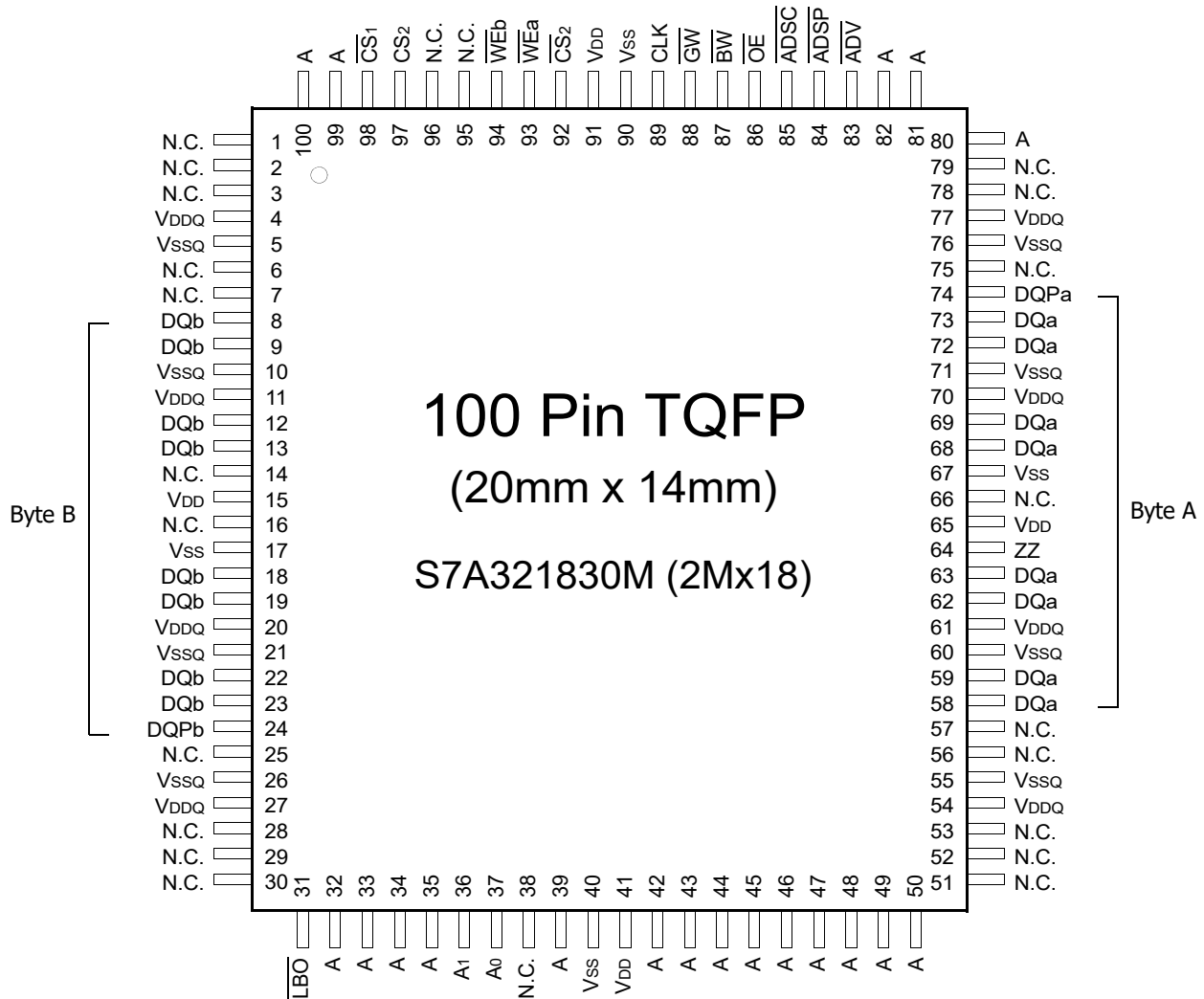
Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,39,42,43,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,66
ADSP	Address Status Processor	84	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
CS2	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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100 TQFP Package Pin Configurations(Top View)



Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,39,42,43,44,45,46,47,48,49,50,80,81,82,99,100	VDD	Power Supply	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29,30,38,51,52,53,56,57,66,75,78,79,95,96
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85			
CLK	Clock	89			
CS1	Chip Select	98	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS2	Chip Select	97	DQb		8,9,12,13,18,19,22,23
CS2	Chip Select	92	DQPa, Pb		74,24
WEx(x=a,b)	Byte Write Inputs	93,94	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

NOTE : A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

165FBGA PKG Pin Configurations - S7A323630M (1Mx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS1}$	\overline{WEc}	\overline{WEb}	$\overline{CS2}$	\overline{BW}	\overline{ADSC}	\overline{ADV}	A	NC
B	NC	A	CS2	\overline{WEd}	\overline{WEa}	CLK	\overline{GW}	\overline{OE}	\overline{ADSP}	A	NC
C	DQP _c	NC	VDDQ	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQP _b
D	DQ _c	DQ _c	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _b	DQ _b
E	DQ _c	DQ _c	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _b	DQ _b
F	DQ _c	DQ _c	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _b	DQ _b
G	DQ _c	DQ _c	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _b	DQ _b
H	NC	NC	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ
J	DQ _d	DQ _d	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _a	DQ _a
K	DQ _d	DQ _d	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _a	DQ _a
L	DQ _d	DQ _d	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _a	DQ _a
M	DQ _d	DQ _d	VDDQ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _a	DQ _a
N	DQP _d	NC	VDDQ	V _{SS}	NC	A	NC	V _{SS}	V _{DDQ}	NC	DQP _a
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	\overline{LBO}	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	VDD	Power Supply
A0,A1	Burst Address Inputs	VSS	Ground
\overline{ADV}	Burst Address Advance	N.C.	No Connect
\overline{ADSP}	Address Status Processor	DQa	Data Inputs/Outputs
\overline{ADSC}	Address Status Controller	DQb	
CLK	Clock	DQc	
$\overline{CS1}$	Chip Select	DQd	
CS2	Chip Select	DQPa~Pd	
$\overline{CS2}$	Chip Select	VDDQ	Output Power Supply
$\overline{WE}(x=a,b,c,d)$	Byte Write Inputs	VSSQ	Output Ground
\overline{OE}	Output Enable		
\overline{GW}	Global Write Enable		
\overline{BW}	Byte Write Enable		
ZZ	Power Down Input		
LBO	Burst Mode Control		

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

165FBGA PKG Pin Configurations - S7A321830M (2Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS1}$	\overline{WEb}	NC	$\overline{CS2}$	\overline{BW}	\overline{ADSC}	\overline{ADV}	A	A
B	NC	A	CS2	NC	\overline{WEa}	CLK	\overline{GW}	\overline{OE}	\overline{ADSP}	A	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQP _a
D	NC	DQ _b	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ _a
E	NC	DQ _b	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ _a
F	NC	DQ _b	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ _a
G	NC	DQ _b	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ _a
H	NC	NC	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQ _b	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ _a	NC
K	DQ _b	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ _a	NC
L	DQ _b	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ _a	NC
M	DQ _b	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ _a	NC
N	DQP _b	NC	VDDQ	Vss	NC	A	NC	Vss	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	\overline{LBO}	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	VDD	Power Supply
A0,A1	Burst Address Inputs	VSS	Ground
\overline{ADV}	Burst Address Advance	N.C.	No Connect
\overline{ADSP}	Address Status Processor	DQ _a	Data Inputs/Outputs
\overline{ADSC}	Address Status Controller	DQ _b	
CLK	Clock	DQP _{a~b}	
$\overline{CS1}$	Chip Select	VDDQ	Output Power Supply
CS2	Chip Select	VSSQ	Output Ground
$\overline{CS2}$	Chip Select		
$\overline{WE}(x=a,b)$	Byte Write Inputs		
\overline{OE}	Output Enable		
\overline{GW}	Global Write Enable		
\overline{BW}	Byte Write Enable		
ZZ	Power Down Input		
\overline{LBO}	Burst Mode Control		

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

S7A323630M S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

Function Description

The S7A323630M and S7A321830M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} . When \overline{ZZ} is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2cycles of wake up time. \overline{ZZ} pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (regardless of \overline{WEx} and \overline{ADSC}) using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of \overline{CLK} , are carried to the Data-out buffer by the next positive edge of \overline{CLK} . The data, registered in the Data-out buffer, are projected to the output pins. \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{WEx} are sampled High and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx}), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low (regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals (\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} control \overline{DQa} and \overline{DQPa} , \overline{WEb} controls \overline{DQb} and \overline{DQPb} , \overline{WEc} controls \overline{DQc} and \overline{DQc} , and \overline{WEd} control \overline{DQd} and \overline{DQPd} . Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

- \overline{ADSP} must be sampled high when \overline{ADSC} is sampled low to initiate a cycle with \overline{ADSC} .
- \overline{WEx} are sampled on the same clock edge that sampled \overline{ADSC} low (and \overline{ADSP} high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

Burst Sequence Table

(Interleaved Burst, \overline{LBO} =High)

\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, \overline{LBO} =Low)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

Asynchronous Truth Table

Operation	\overline{ZZ}	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. \overline{ZZ} pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

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Truth Tables

Synchronous Truth Table

\overline{CS}_1	CS_2	\overline{CS}_2	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{Write}	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :**
1. X means "Don't Care".
 2. The rising edge of clock is symbolized by (↑).
 3. $\overline{Write} = L$ means Write operation in Write Truth Table.
 $\overline{Write} = H$ means Read operation in Write Truth Table.
 4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

Write Truth Table(x36)

\overline{GW}	\overline{BW}	\overline{WEa}	\overline{WEb}	\overline{WEc}	\overline{WEd}	OPERATION
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte A
H	L	H	L	H	H	Write Byte B
H	L	H	H	L	L	Write Byte C And D
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

- Notes :**
1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Write Truth Table(x18)

\overline{GW}	\overline{BW}	\overline{WEa}	\overline{WEb}	OPERATION
H	H	X	X	Read
H	L	H	H	Read
H	L	L	H	Write Byte A
H	L	H	L	Write Byte B
H	L	L	L	Write All Bytes
L	X	X	X	Write All Bytes

- Notes :**
1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.3 to 4.6	V	
Voltage on V _{DDQ} Supply Relative to V _{SS}	V _{DDQ}	V _{DD}	V	
Voltage on Input Pin Relative to V _{SS}	V _{IN}	-0.3 to V _{DD} +0.3	V	
Voltage on I/O Pin Relative to V _{SS}	V _{IO}	-0.3 to V _{DDQ} +0.3	V	
Power Dissipation	P _D	1.6	W	
Storage Temperature	T _{STG}	-65 to 150	°C	
Operating Temperature	Commercial	T _{OPR}	0 to 70	°C
	Industrial	T _{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias	T _{BIAS}	-10 to 85	°C	

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{DD1}	1.7	1.8	2.0	V
	V _{DDQ1}	1.7	1.8	2.0	V
	V _{DD2}	2.3	2.5	2.7	V
	V _{DDQ2}	1.7	2.5	2.7	V
	V _{DD3}	3.1	3.3	3.5	V
	V _{DDQ3}	2.3	3.3	3.5	V
Ground	V _{SS}	0	0	0	V

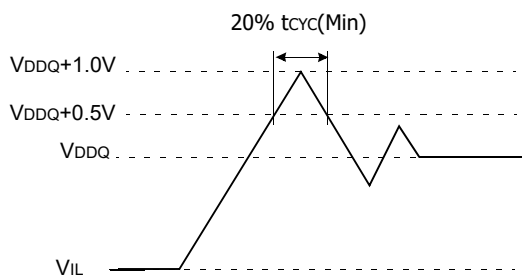
Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$

Capacitance (T_A=25°C, f=1MHz)

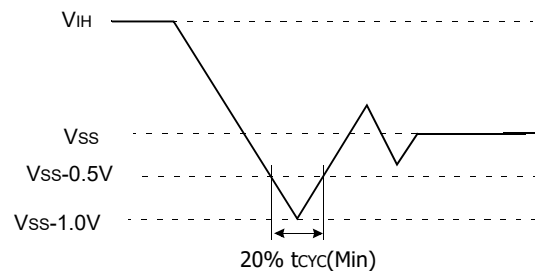
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes	
Input Leakage Current(except	I _{IL}	V _{DD} =Max ; V _{IN} =V _{SS} to V _{DD}	-2	+2	uA		
Output Leakage Current	I _{OL}	Output Disabled, V _{out} =V _{SS} to V _{DDQ}	-2	+2	uA		
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ ≤ V _{IL} , Cycle Time ≥ t _{cyc} Min	-25	-	300	mA	1,2
			-16	-	260		
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ ≤ V _{IL} , f=Max, All Inputs ≤ V _{IL} or ≥ V _{IH}	-25	-	150	mA	
			-16	-	145		
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	-	120	mA	
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ ≥ V _{DD} -0.2V, f=Max, All Inputs ≤ V _{IL} or ≥ V _{IH}	-	-	120		
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V		
Output Low Voltage(1.8V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V		
Output High Voltage(1.8V I/O)	V _{OH}	I _{OH} =-1.0mA	V _{DDQ} -0.4	-	V		
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.3**	V	3	
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.3**	V	3	
Input Low Voltage(1.8V I/O)	V _{IL}		-0.3*	V _{DD} x 0.3	V		
Input High Voltage(1.8V I/O)	V _{IH}		V _{DD} x 0.6	V _{DD} +0.3**	V	3	

Notes : The above parameters are also guaranteed at industrial temperature range.
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

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1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

Test Conditions

Parameter	Value
Input Pulse Level for 3.3V I/O	0 to 3.0V
Input Pulse Level for 2.5V I/O	0 to 2.5V
Input Pulse Level for 1.8V I/O	0 to 1.8V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O and 1.8V I/O	V _{DDQ} /2
Output Load	See Fig. 1

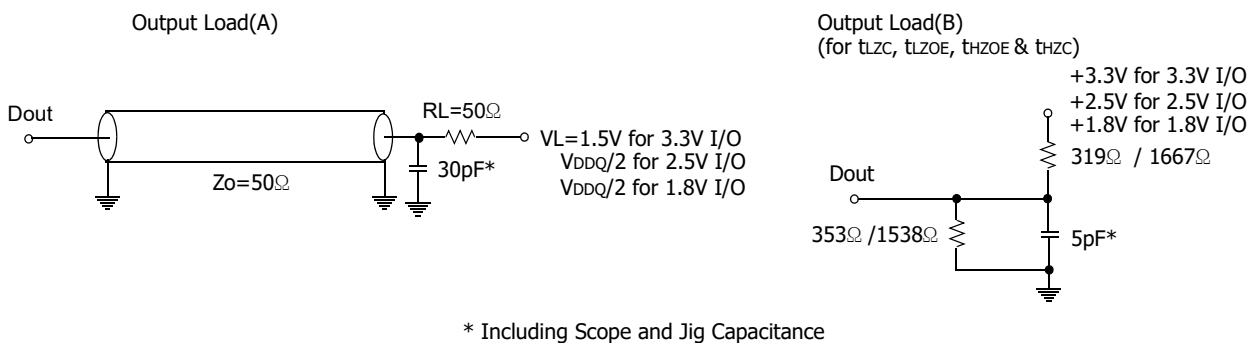


Fig. 1

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AC Timing Characteristics

Parameter	Symbol	-25		-16		Unit
		Min	Max	Min	Max	
Cycle Time	t _{CYC}	4.0	-	6.0	-	ns
Clock Access Time (V _{dd} =2.5V and 3.3V)	t _{CD}	-	2.6	-	3.5	ns
Clock Access Time (V _{dd} =1.8V)		-	3.0	-	3.5	ns
Output Enable to Data Valid (V _{dd} =2.5V and 3.3V)	t _{OE}	-	2.6	-	3.5	ns
Output Enable to Data Valid (V _{dd} =1.8V)		-	3.0	-	3.5	ns
Clock High to Output Low-Z	t _{LZC}	1.5	-	1.5	-	ns
Output Hold from Clock High	t _{OH}	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	2.6	-	3.0	ns
Clock High to Output High-Z	t _{HZC}	-	2.6	-	3.0	ns
Clock High Pulse Width	t _{CH}	1.7	-	2.2	-	ns
Clock Low Pulse Width	t _{CL}	1.7	-	2.2	-	ns
Address Setup to Clock High	t _{AS}	1.2	-	1.5	-	ns
Address Status Setup to Clock High	t _{SS}	1.2	-	1.5	-	ns
Data Setup to Clock High	t _{DS}	1.2	-	1.5	-	ns
Write Setup to Clock High (\overline{WE} , \overline{BWx})	t _{WS}	1.2	-	1.5	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.2	-	1.5	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.2	-	1.5	-	ns
Address Hold from Clock High	t _{AH}	0.3	-	0.5	-	ns
Address Status Hold from Clock High	t _{SH}	0.3	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.3	-	0.5	-	ns
Write Hold from Clock High (\overline{WE} , \overline{BWx})	t _{WH}	0.3	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.3	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.3	-	0.5	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	cycle

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
 2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever \overline{ADSC} and/or \overline{ADSP} is sampled low and \overline{CS} is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 3. Both chip selects must be active whenever \overline{ADSC} or \overline{ADSP} is sampled low in order for the this device to remain enabled.
 4. \overline{ADSC} or \overline{ADSP} must not be asserted for at least 2 Clock after leaving ZZ state.

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Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.

After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.

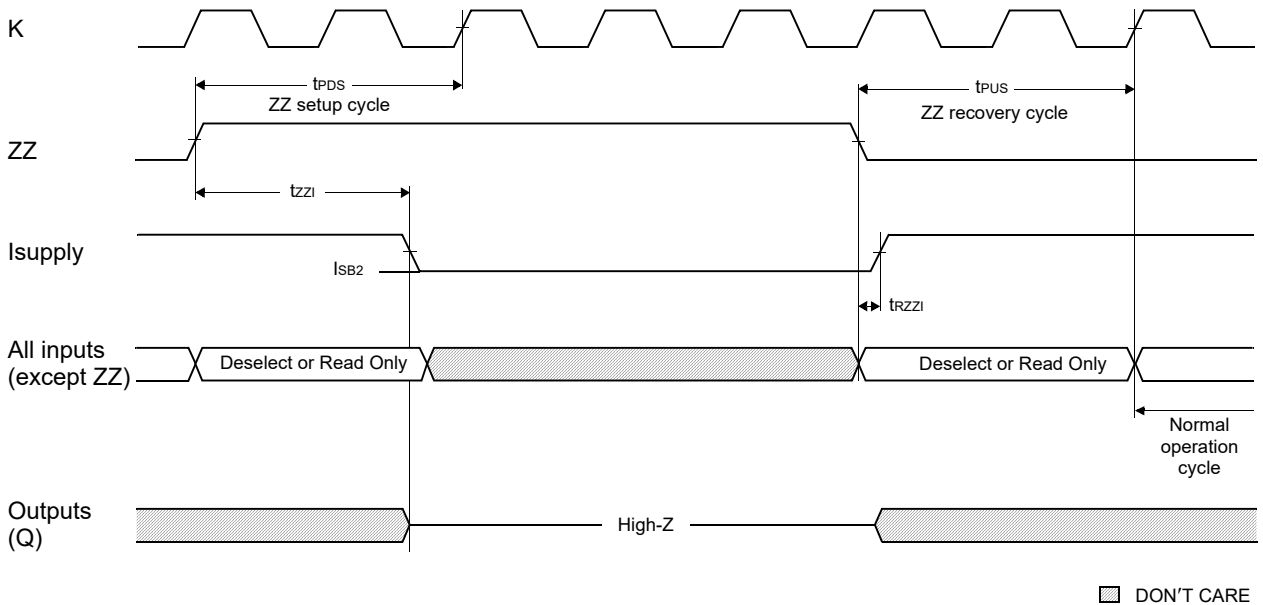
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep Mode during t_{PUS} , only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

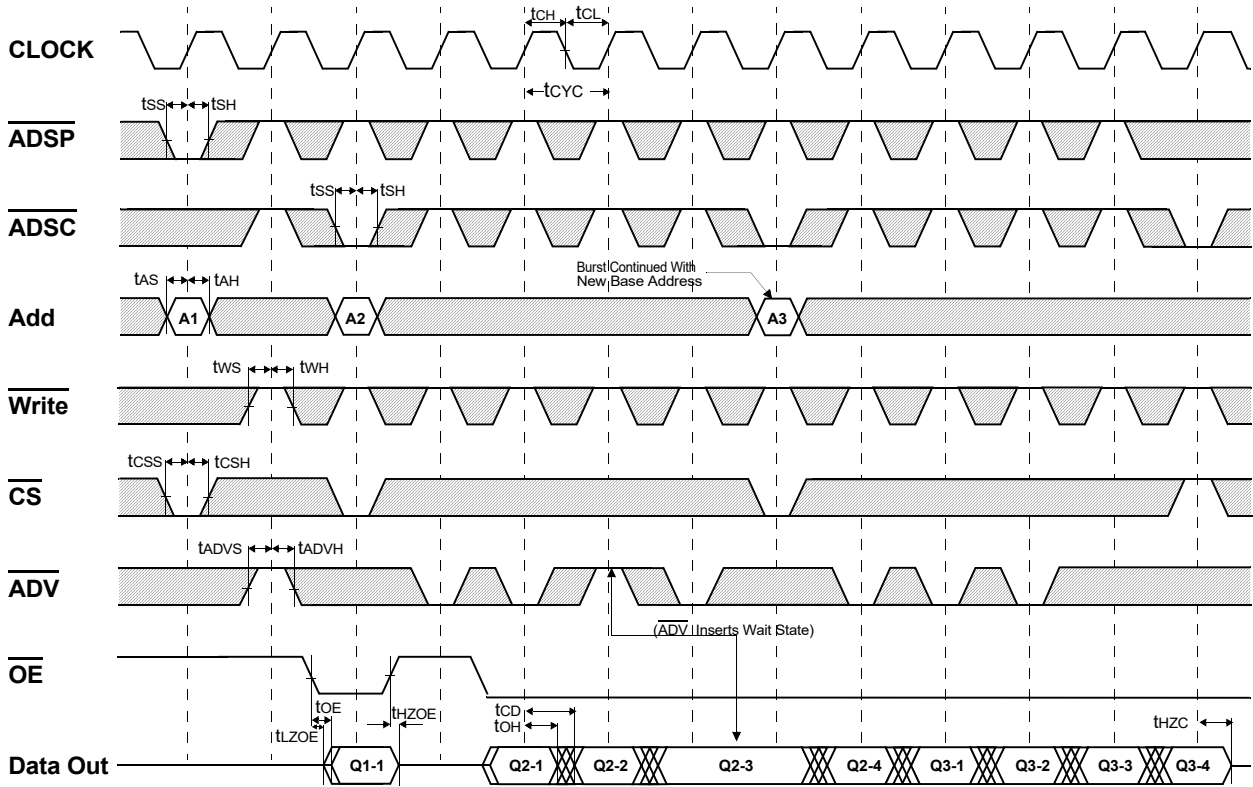
Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		120	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

Sleep Mode Waveform



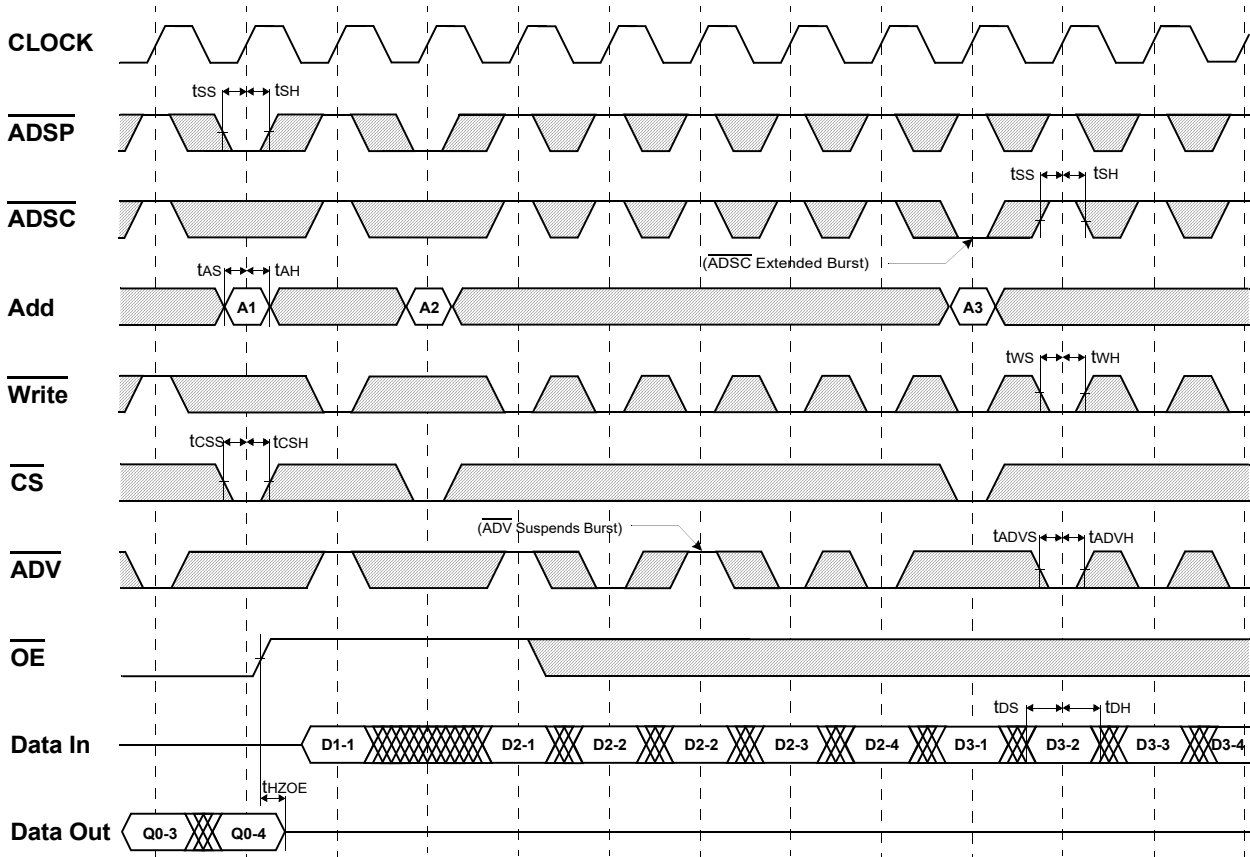
Timing Waveform of Read Cycle



NOTES: $\overline{\text{Write}} = L$ means $\text{GW} = L$, or $\text{GW} = H$, $\text{BW} = L$, $\text{WEX} = L$
 $\overline{\text{CS}} = L$ means $\text{CS}_1 = L$, $\text{CS}_2 = H$ and $\overline{\text{CS}}_2 = L$
 $\overline{\text{CS}} = H$ means $\overline{\text{CS}}_1 = H$, or $\overline{\text{CS}}_1 = L$ and $\overline{\text{CS}}_2 = H$, or $\overline{\text{CS}}_1 = L$, and $\text{CS}_2 = L$

□ Don't Care
 X Undefined

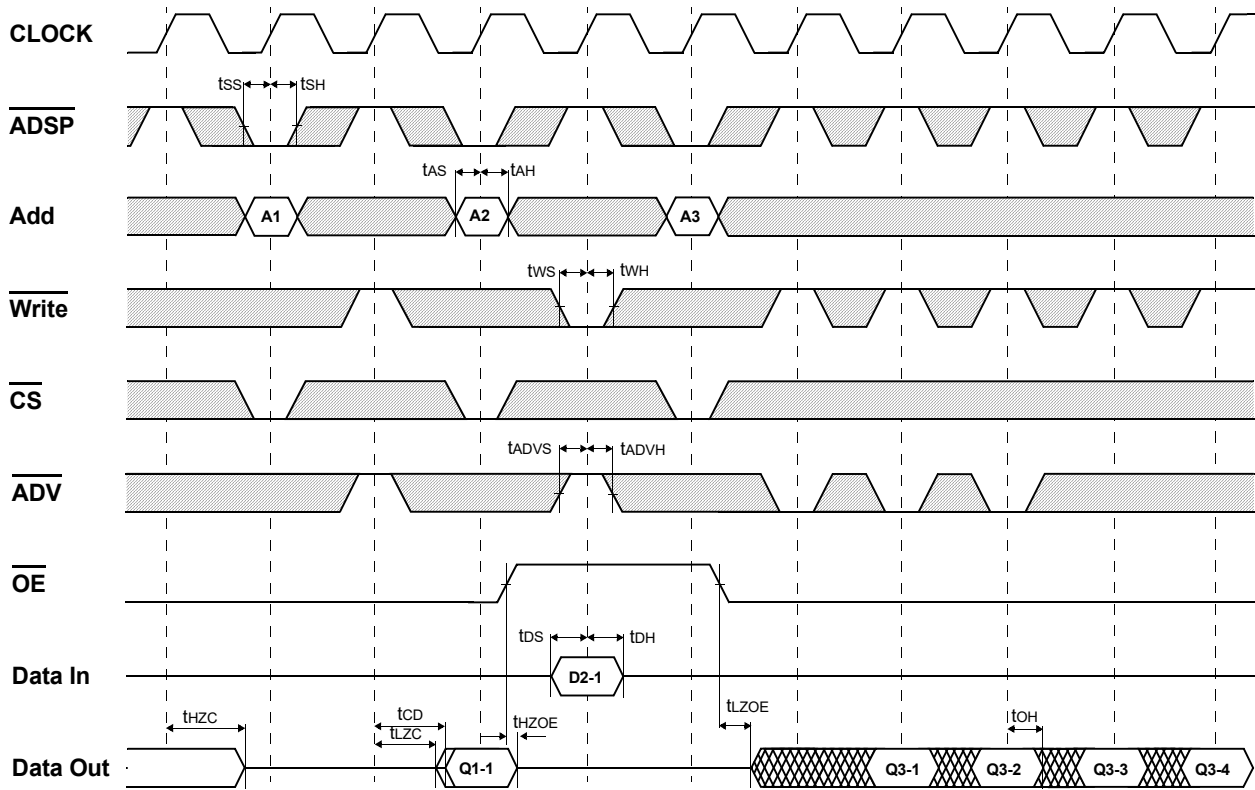
Timing Waveform of Write Cycle



NOTES: $\overline{\text{Write}} = \text{L}$ means $\text{GW} = \text{L}$, or $\text{GW} = \text{H}$, $\text{BW} = \text{L}$, $\text{WEX} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\text{CS}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\text{CS}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\text{CS}_1 = \text{H}$, or $\text{CS}_1 = \text{L}$ and $\text{CS}_2 = \text{H}$, or $\text{CS}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

□ Don't Care
 ⊠ Undefined

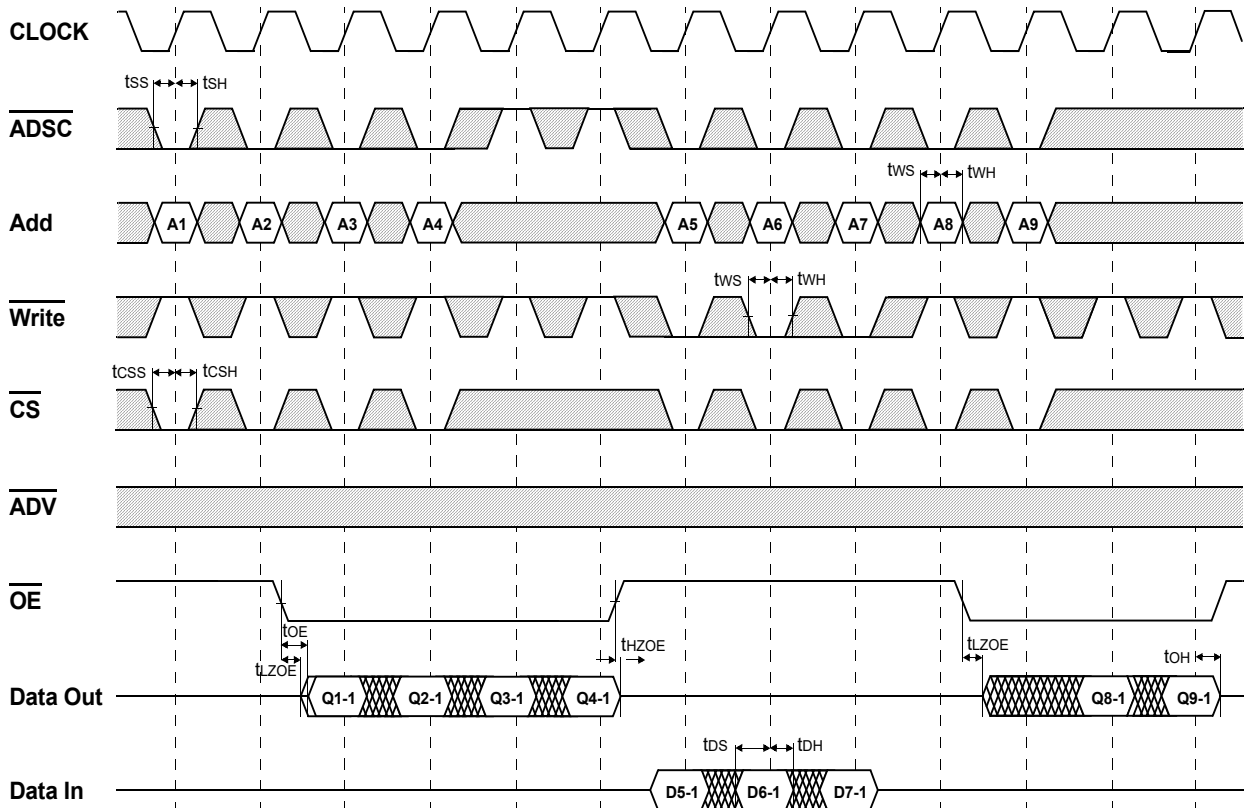
Timing Waveform of Combination Read/Write Cycle(ADSP Controlled , ADSC=High)



NOTES: $\overline{\text{Write}} = \text{L}$ means $\overline{\text{GW}} = \text{L}$, or $\overline{\text{GW}} = \text{H}$, $\overline{\text{BW}} = \text{L}$, $\overline{\text{WEX}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

□ Don't Care
 ▣ Undefined

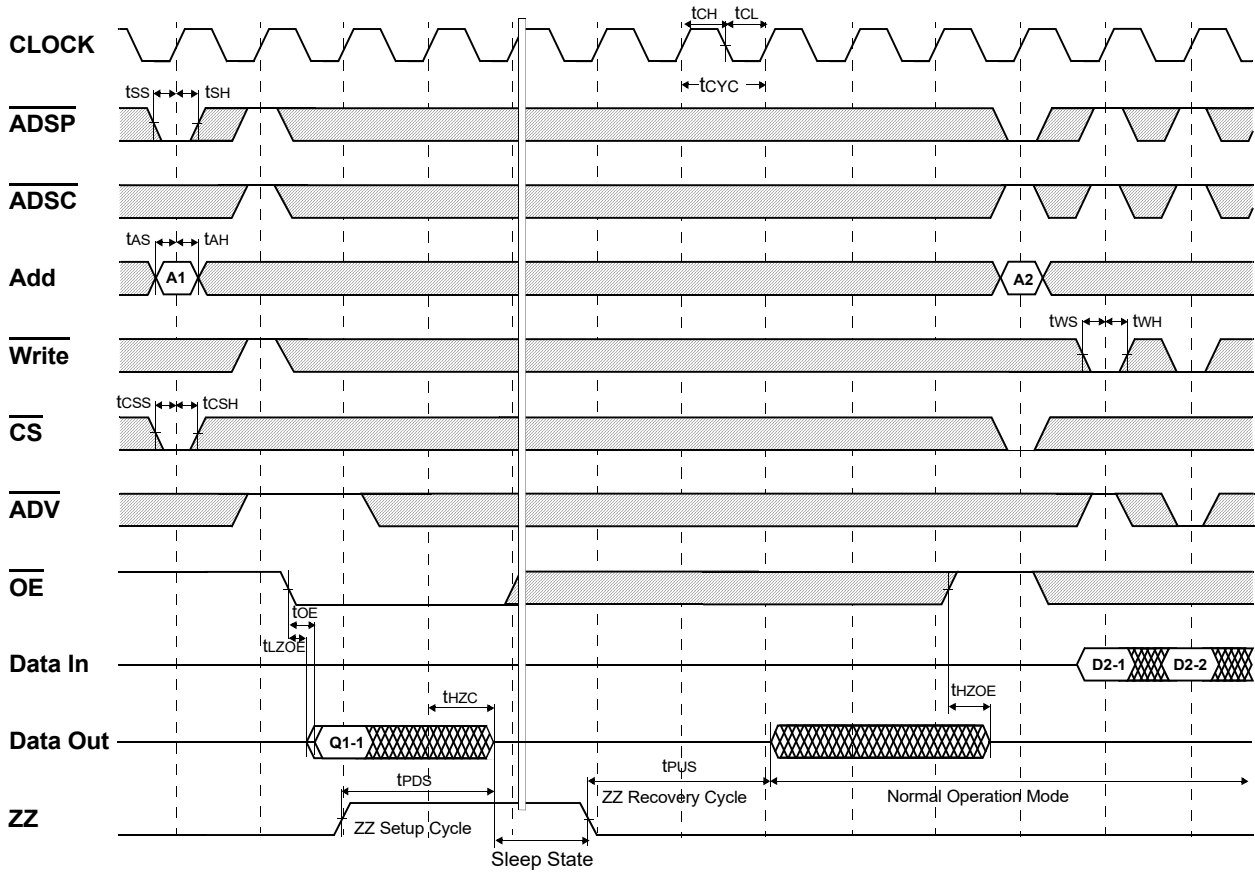
Timing Waveform of Single Read/Write Cycle ($\overline{\text{ADSC}}$ Controlled, $\overline{\text{ADSP}}=\text{High}$)



NOTES: $\overline{\text{Write}} = \text{L}$ means $\text{GW} = \text{L}$, or $\text{GW} = \text{H}$, $\text{BW} = \text{L}$, $\text{WEX} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

▨ Don't Care
 ▩ Undefined

Timing Waveform of Power Down Cycle



NOTES: $\overline{\text{Write}} = \text{L}$ means $\text{GW} = \text{L}$, or $\text{GW} = \text{H}$, $\text{BW} = \text{L}$, $\text{WEx} = \text{L}$
 $\text{CS} = \text{L}$ means $\text{CS}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\text{CS}_2 = \text{L}$
 $\text{CS} = \text{H}$ means $\text{CS}_1 = \text{H}$, or $\text{CS}_1 = \text{L}$ and $\text{CS}_2 = \text{H}$, or $\text{CS}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

□ Don't Care
 ▨ Undefined

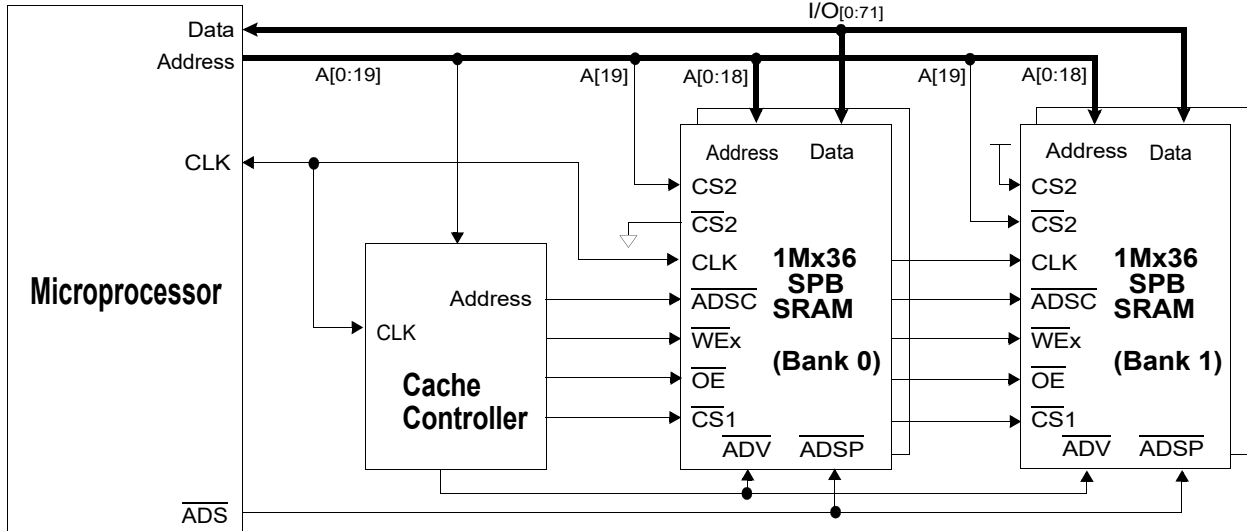
S7A323630M S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

Application Information

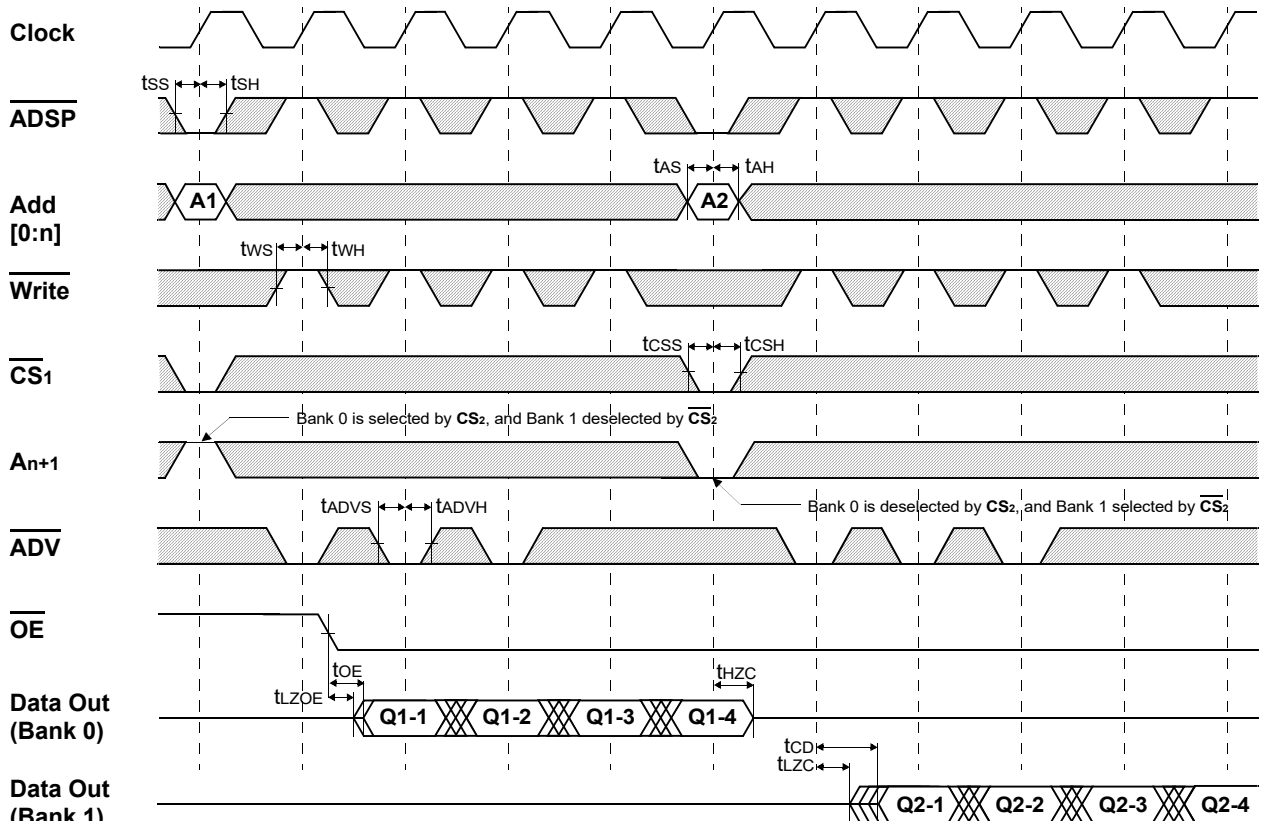
Depth Expansion

The Netsol 1Mx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

(ADSP Controlled, ADSC=High)



*Notes : n = 14 32K depth, 15 64K depth
 16 128K depth, 17 256K depth
 18 512K depth, 19 1M depth
 20 2M depth

□ Don't Care ⊗ Undefined



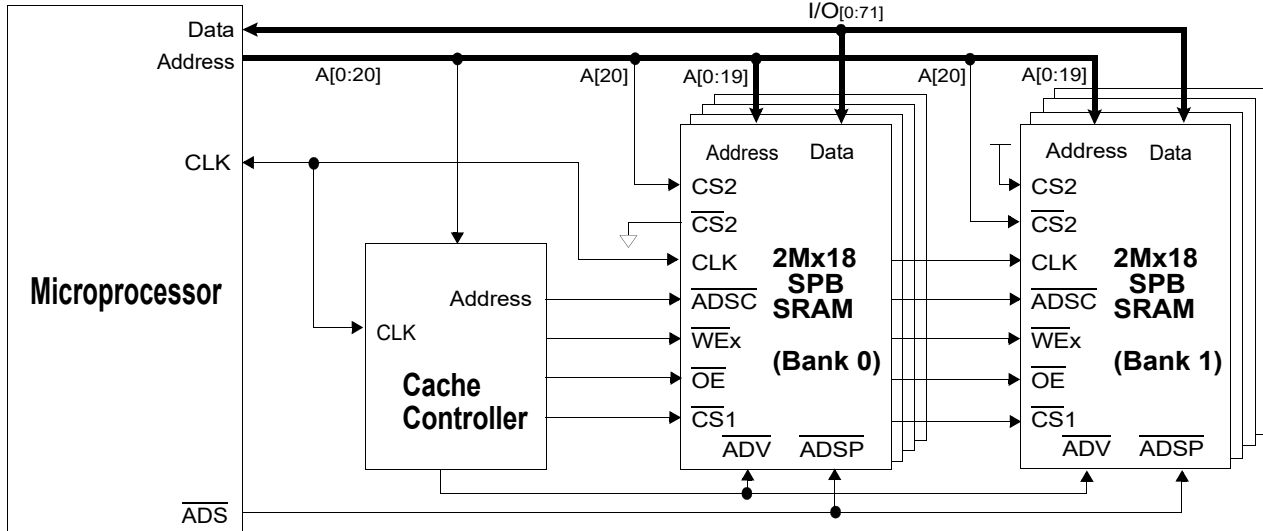
S7A323630M S7A321830M

1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

Application Information

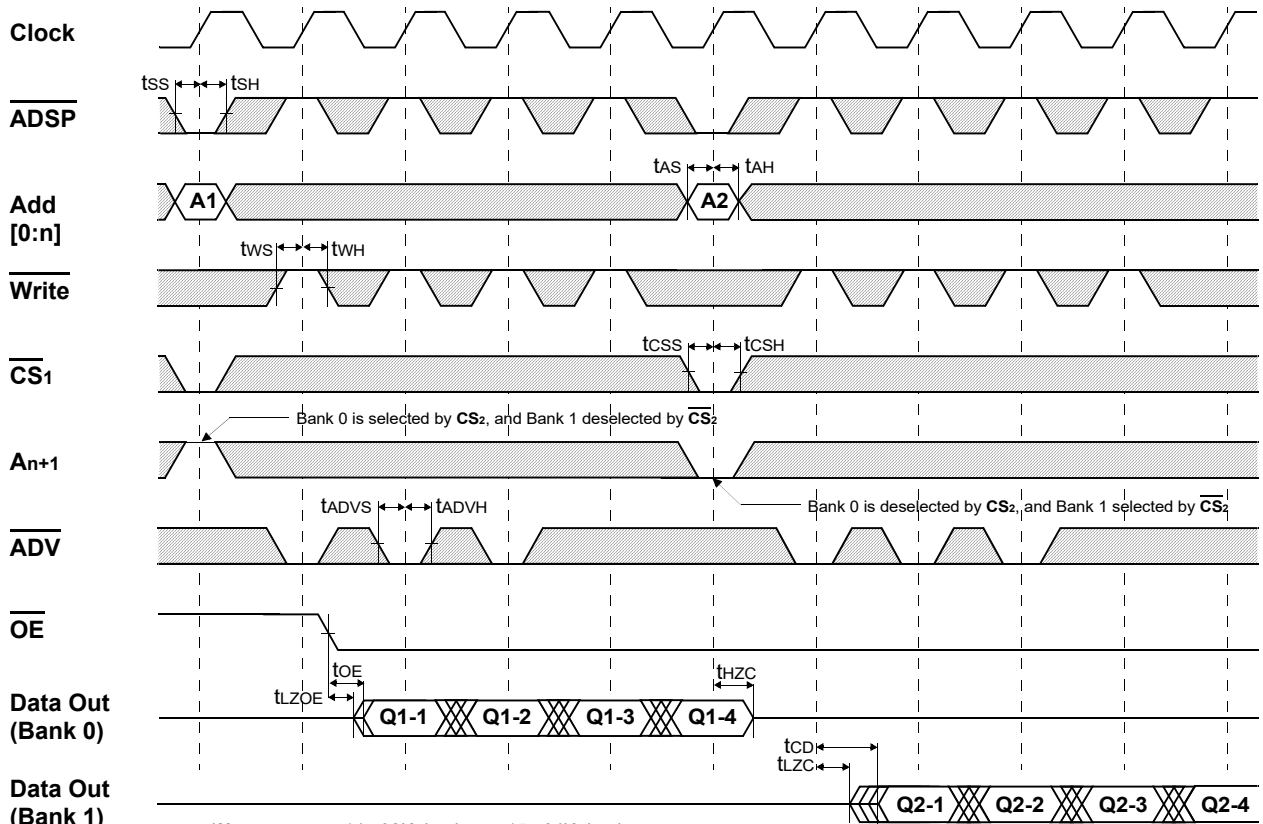
Depth Expansion

The Netsol 2Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 2M depth to 4M depth without extra logic.



Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

(ADSP Controlled, ADSC=High)



*Notes : n = 14 32K depth, 15 64K depth
 16 128K depth, 17 256K depth
 18 512K depth, 19 1M depth
 20 2M depth, 21 4M depth

□ Don't Care ⊗ Undefined

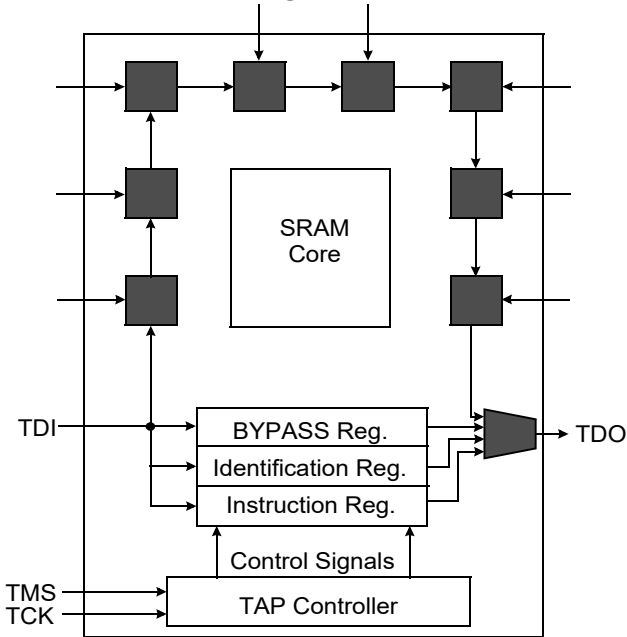
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1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



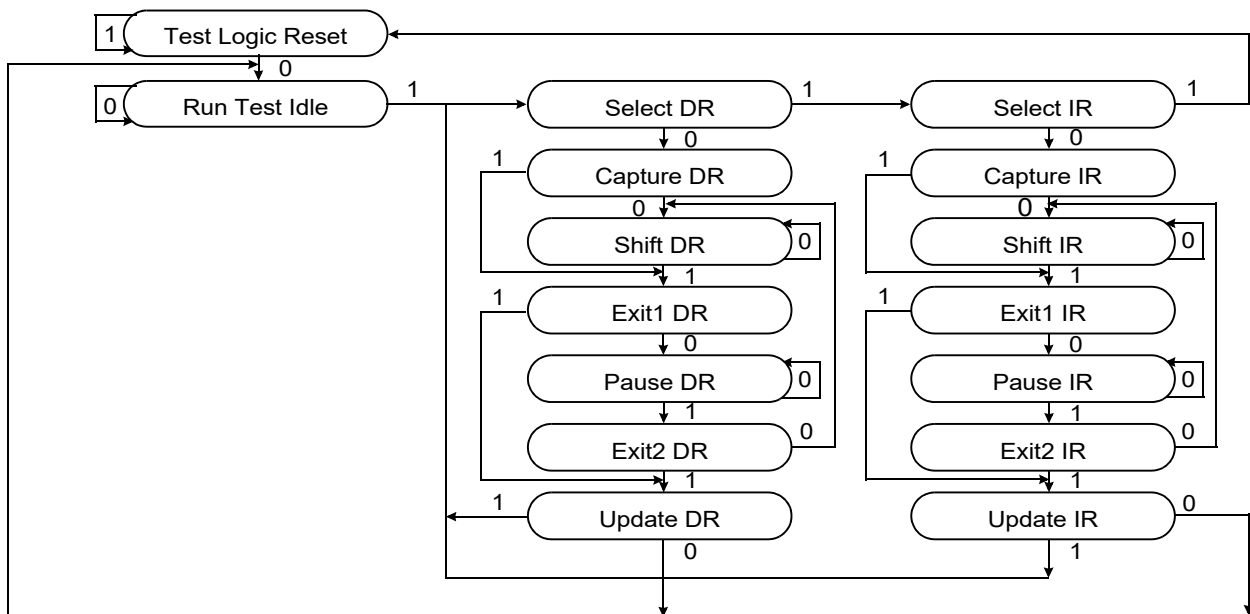
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE:

- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
- Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
- TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
- Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
- SAMPLE instruction dose not places DQs in Hi-Z.
- This instruction is reserved for future use.

TAP Controller State Diagram



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Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36 2M x 18	3 bits	1 bit	32 bits	76 bits

ID Registration Definition

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
1M x 36	0000	01000 00100	000000	01111011001	1
2M x 18	0000	01001 00011	000000	01111011001	1

Boundary Scan Exit Order

BIT	Pin ID (x18)	Pin ID (x36)
1	6N	6N
2	8P	8P
3	8R	8R
4	9R	9R
5	9P	9P
6	10P	10P
7	10R	10R
8	11R	11R
9	11P	11P
10	11H	11H
11	11N	11N
12	11M	11M
13	11L	11L
14	11K	11K
15	11J	11J
16	10M	10M
17	10L	10L
18	10K	10K
19	10J	10J
20	11G	11G
21	11F	11F
22	11E	11E
23	11D	11D
24	11C	10G
25	10F	10F
26	10E	10E
27	10D	10D
28	10G	11C
29	11A	11A
30	11B	11B
31	10A	10A
32	10B	10B
33	9A	9A
34	9B	9B
35	8A	8A
36	8B	8B
37	7A	7A
38	7B	7B
39	6B	6B

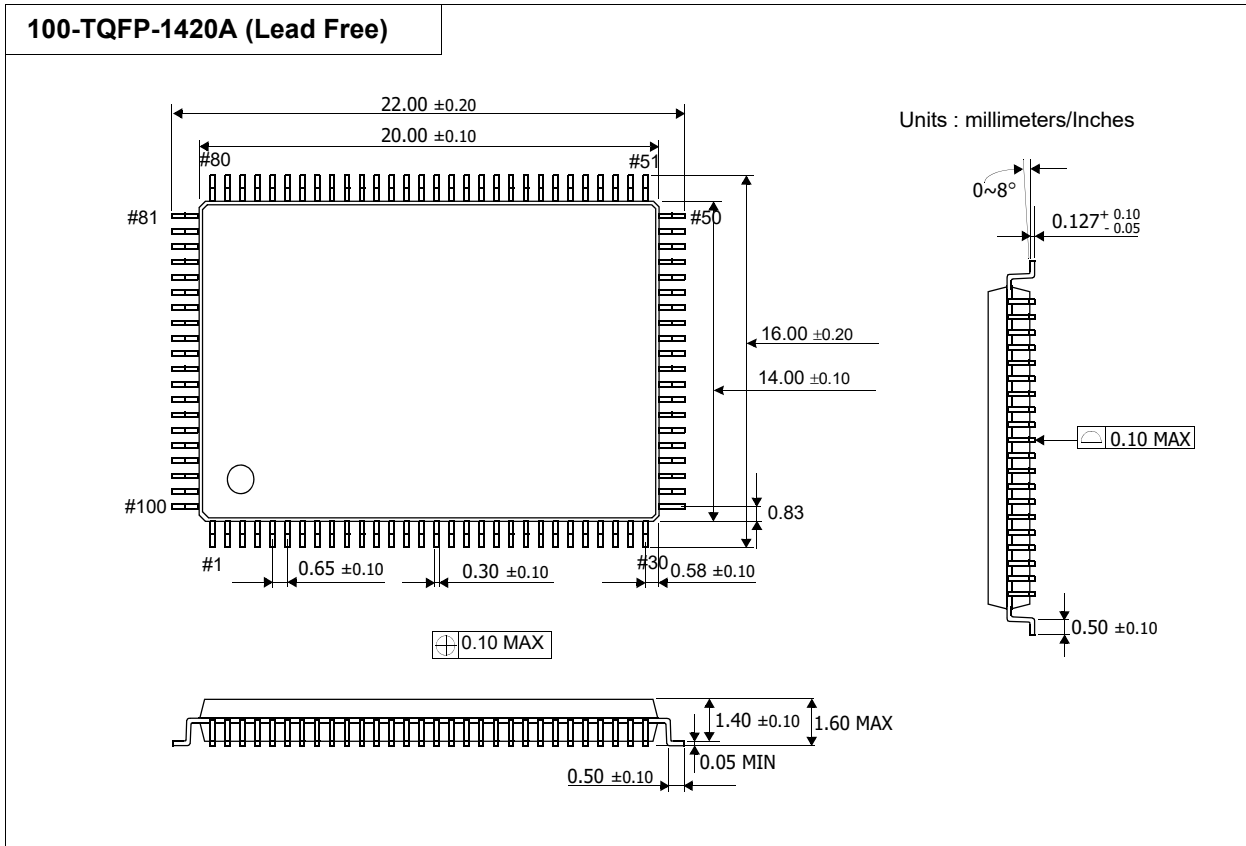
BIT	Pin ID (x18)	Pin ID (x36)
40	6A	6A
41	5B	5B
42	5A	5A
43	4A	4A
44	4B	4B
45	3B	3B
46	3A	3A
47	2A	2A
48	2B	2B
49	1B	1B
50	1A	1A
51	1C	1C
52	1D	1D
53	1E	1E
54	1F	1F
55	1G	1G
56	2D	2D
57	2E	2E
58	2F	2F
59	2G	2G
60	1J	1J
61	1K	1K
62	1L	1L
63	1M	1M
64	1N	2J
65	2K	2K
66	2L	2L
67	2M	2M
68	2J	1N
69	2R	2R
70	1R	1R
71	3P	3P
72	3R	3R
73	4R	4R
74	4P	4P
75	6P	6P
76	6R	6R

Note: 1. NC pins are read as "X" (i.e. don't care.)

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1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

Package Dimensions

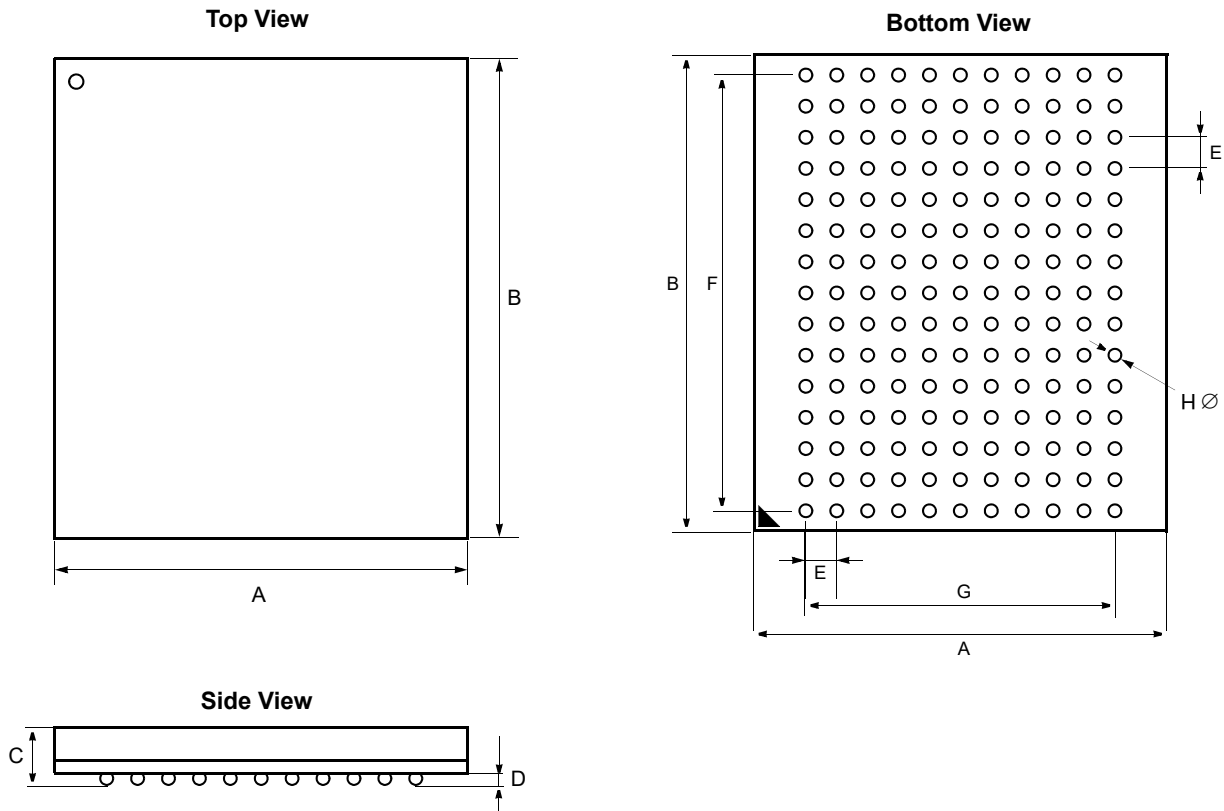


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1Mx36 & 2Mx18 Sync-Pipelined Burst SRAM

165 FBGA Package Dimensions (Lead Free)

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		E	1.0	mm	
B	15 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.5 ± 0.05	mm	