18Mb Quadruple BL2
SRAM Specification

165FBGA with Pb & Pb Free
(ROHS Compliant)

Document Title

512Kx36 & 1Mx18 - Bit Quadruple Burst Length of 2 SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 2012	Preliminary
1.0	Final spec release	Feb. 2013	Final
1.1	Change Thermal Resistance θJA value from 20.8°C/W to 16.3°C/W	Apr. 2013	Final

512Kx36 & 1Mx18 - Bit Quadruple Burst Length of 2 SRAM

Features

- 1.8V/2.5V +0.1V/-0.1V Power Supply.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O,
  1.8V+0.1V/-0.1V for 1.8V I/O.
- Separate independent read and write data ports
  with concurrent read and write operation
- HSTL I/O
- Full data coherency, providing most current data.
- Synchronous pipeline read with self timed early write.
- Registered address, control and data input/output.
- DDR (Double Data Rate) Interface on read and write ports.
- Fixed 2-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks (K and $\overline{K}$) for accurate DDR timing at clock
  rising edges only.
- Two input clocks for output data (C and $\overline{C}$) to minimize
  clock-skew and flight-time mismatches.
- Single address bus.
- Byte write (x18, x36) function.
- Separate read/write control pin ($\overline{R}$ and $\overline{W}$)
- Simple depth expansion with no data contention.
- Programmable output impedance.
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball array FBGA) with body size of 13x15mm
  & Lead Free

Key Parameters

Part Number	Org.	Cycle Time	Access Time	Unit	RoHS
S7Q163662M-E(F)C(I)16	X36	6.0	2.5	ns	O
S7Q161862M-E(F)C(I)16	X18	6.0	2.5	ns	O

* -E(F)C(I)
   E(F) [Package type]: E-Pb Free, F-Pb
   C(I) [Operating Temperature]: C-Commercial, I-Industrial

GENERAL DESCRIPTION

The S7Q163662M and S7Q161862M are 18,874,368-bits Quadruple Synchronous Pipelined Burst SRAMs. They are organized as 524,288 words by 36bits for S7Q163662M and 1,048,576 words by 18bits for S7Q161862M.

The Quadruple operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of K and $\overline{K}$, and transferred out of SRAM on every rising edge of C and $\overline{C}$. And totally independent read and write ports eliminate the need for high speed bus turn around.

Address, data inputs, and all control signals are synchronized to the input clock (K or $\overline{K}$). Normally data outputs are synchronized to output clocks (C and $\overline{C}$), but when C and $\overline{C}$ are tied high, the data outputs are synchronized to the input clocks (K and $\overline{K}$).

Read address is registered on rising edges of the input K clocks, and write address is registered on rising edges of the input $\overline{K}$ clocks. Common address bus is used to access address both for read and write operations. The internal burst counter is fixed to 2-bit sequential for both read and write operations. Synchronous pipeline read and early write enable high speed operations. Simple depth expansion is accomplished by using $\overline{R}$ and $\overline{W}$ for port selection. Byte write operation is supported with $\overline{BW}_0$ and $\overline{BW}_1$ ($\overline{BW}_2$ and $\overline{BW}_3$) pins for x18 (x36) device.
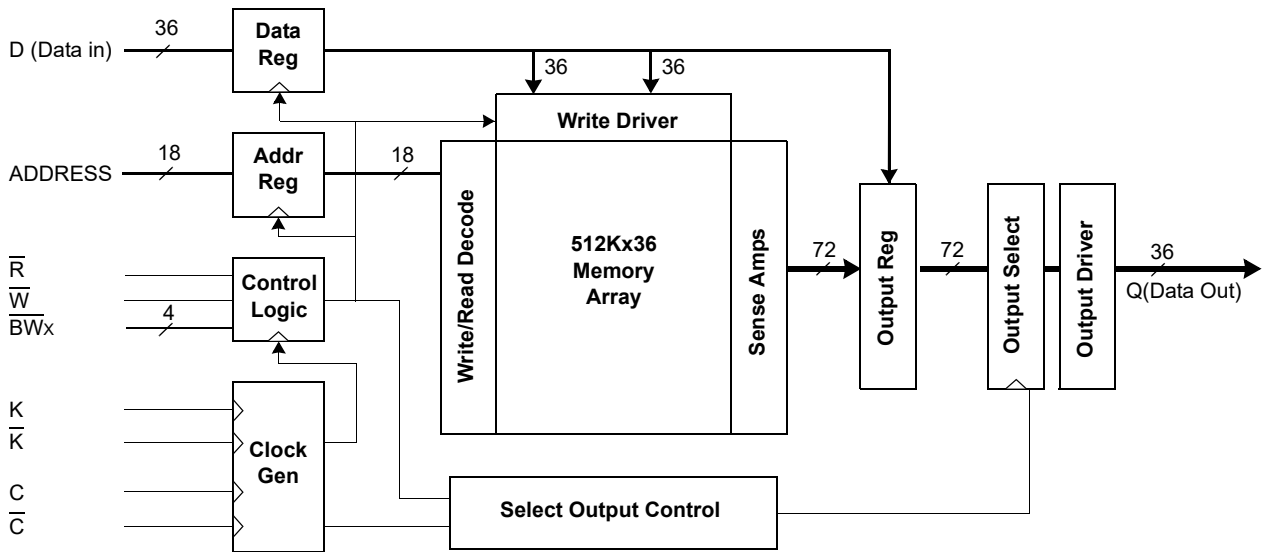
IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoring package pads attachment status with system.

The S7Q163662M and S7Q161862M are implemented with Netsol's high performance 6T CMOS technology and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.
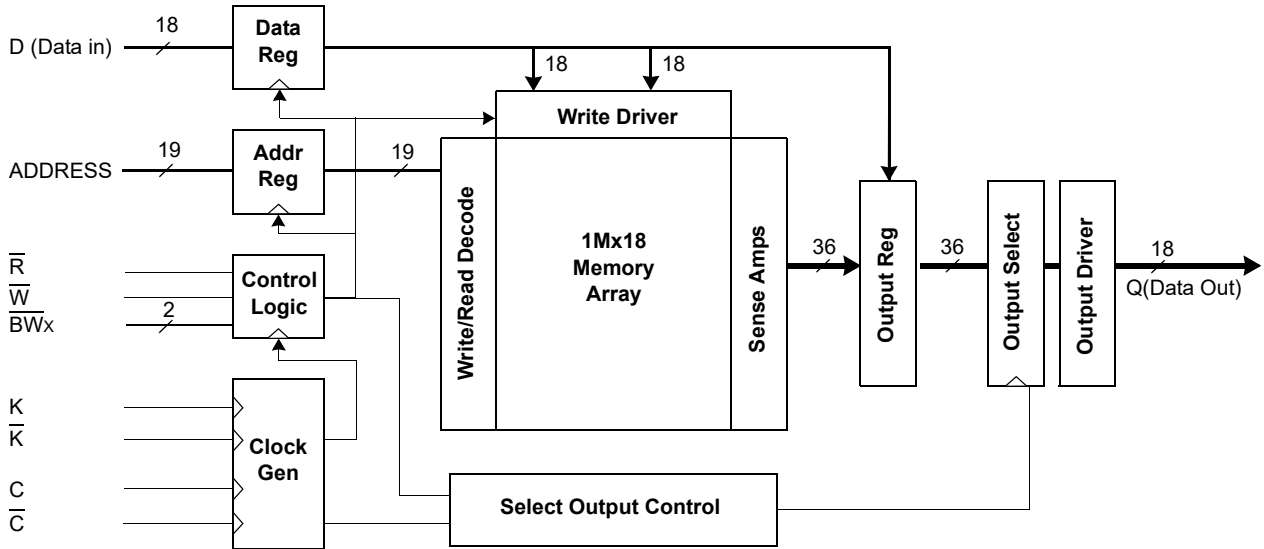
NETSOL

Logic Block Diagram - S7Q163662M (512K x 36)

Logic Block Diagram - S7Q161862M (1M x 18)

165FBGA PKG Pin Configurations - S7Q163662M (512Kx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	Vss	NC	$\overline{W}$	$\overline{BW}_2$	$\overline{K}$	$\overline{BW}_1$	$\overline{R}$	NC	Vss	NC
B	Q27	Q18	D18	SA	$\overline{BW}_3$	K	$\overline{BW}_0$	SA	D17	Q17	Q8
C	D27	Q28	D19	Vss	SA	SA	SA	Vss	D16	Q7	D8
D	D28	D20	Q19	Vss	Vss	Vss	Vss	Vss	Q16	D15	D7
E	Q29	D29	Q20	VDDQ	Vss	Vss	Vss	VDDQ	Q15	D6	Q6
F	Q30	Q21	D21	VDDQ	VDD	Vss	VDD	VDDQ	D14	Q14	Q5
G	D30	D22	Q22	VDDQ	VDD	Vss	VDD	VDDQ	Q13	D13	D5
H	NC	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	D31	Q31	D23	VDDQ	VDD	Vss	VDD	VDDQ	D12	Q4	D4
K	Q32	D32	Q23	VDDQ	VDD	Vss	VDD	VDDQ	Q12	D3	Q3
L	Q33	Q24	D24	VDDQ	Vss	Vss	Vss	VDDQ	D11	Q11	Q2
M	D33	Q34	D25	Vss	Vss	Vss	Vss	Vss	D10	Q1	D2
N	D34	D26	Q25	Vss	SA	SA	SA	Vss	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1.$\overline{BW}_0$ controls write to D0:D8, $\overline{BW}_1$ controls write to D9:D17, $\overline{BW}_2$ controls write to D18:D26 and $\overline{BW}_3$ controls write to D27:D35.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
SA	4B,8B,5C-7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-35	10P,11N,11M,10K,11J,11G,10E,11D,11C,10N,9M,9L, 9J,10G,9F,10D,9C,9B,3B,3C,2D,3F,2G,3J,3L,3M,2N, 1C,1D,2E,1G,1J,2K,1M,1N,2P	Data Inputs	
Q0-35	11P,10M,11L,11K,10J,11F,11E,10C,11B,9P,9N,10L, 9K,9G,10F,9E,9D,10B,2B,3D,3E,2F,3G,3K,2L,3N, 3P,1B,2C,1E,1F,2J,1K,1L,2M,1P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW}_0$,$\overline{BW}_1$,$\overline{BW}_2$,$\overline{BW}_3$	7B,7A,5A,5B	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (2.5V)	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
Vss	2A,10A,4C,8C,4D-8D,5E-7E, 6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	1A,3A,9A,11A,1H	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to VREF voltage.

   2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.

   3. Not connected to chip pad internally.

165FBGA PKG Pin Configurations - S7Q161862M (1Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	Vss	NC	$\overline{W}$	$\overline{BW}_1$	$\overline{K}$	NC	$\overline{R}$	SA	Vss	NC
B	NC	Q9	D9	SA	NC	K	$\overline{BW}_0$	SA	NC	NC	Q8
C	NC	NC	D10	Vss	SA	SA	SA	Vss	NC	Q7	D8
D	NC	D11	Q10	Vss	Vss	Vss	Vss	Vss	NC	NC	D7
E	NC	NC	Q11	VDDQ	Vss	Vss	Vss	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	D5
H	NC	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	Vss	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q2
M	NC	NC	D16	Vss	Vss	Vss	Vss	Vss	NC	Q1	D2
N	NC	D17	Q16	Vss	SA	SA	SA	Vss	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1.$\overline{BW}_0$ controls write to D0:D8 and $\overline{BW}_1$ controls write to D9:D17.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
SA	9A,4B,8B,5C-7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-17	10P,11N,11M,10K,11J,11G,10E,11D,11C,3B,3C,2D, 3F,2G,3J,3L,3M,2N	Data Inputs	
Q0-17	11P,10M,11L,11K,10J,11F,11E,10C,11B,2B,3D,3E, 2F,3G,3K,2L,3N,3P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW}_0$, $\overline{BW}_1$	7B, 5A	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (2.5V)	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
Vss	2A,10A,4C,8C,4D-8D,5E-7E, 6F,6G,6H,6J,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	1A,3A,7A,11A,1B,5B,9B,10B,1C,2C,9C,1D,9D, 10D,1E,2E,9E,1F,9F,10F,1G,9G,10G,1H,1J,2J,9J,1K, 2K,9J,1L,9L,10L,1M,2M,9M,1N,9N,10N,1P,2P,9P	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to VREF voltage.
    2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
    3. Not connected to chip pad internally.

Read Operations

Read cycles are initiated by activating $\overline{R}$ at the rising edge of the positive input clock K. Address is presented and stored in the read address register synchronized with K clock. For 2-bit burst DDR operation, it will access two 36-bit or 18-bit data words with each read command. The first pipelined data is transferred out of the device triggered by C clock following next K clock rising edge. Next burst data is triggered by the rising edge of following $\overline{C}$ clock rising edge. Continuous read operations are initiated with K clock rising edge. And pipelined data are transferred out of device on every rising edge of both C and $\overline{C}$ clocks. In case C and $\overline{C}$ tied to high, output data are triggered by K and $\overline{K}$ instead of C and $\overline{C}$. When the $\overline{R}$ is disabled after a read operation, the S7Q163662M and S7Q161862M will first complete burst read operation before entering into deselect mode at the next K clock rising edge. Then output drivers disabled automatically to high impedance state.

Write Operations

Write cycles are initiated by activating $\overline{W}$ at the rising edge of the positive input clock K. Address is presented and stored in the write address register synchronized with following $\overline{K}$ clock. For 2-bit burst DDR operation, it will write two 36-bit or 18-bit data words with each write command. The first "early" data is transferred and registered in to the device synchronous with same K clock rising edge with $\overline{W}$ presented. Next burst data is transferred and registered synchronous with following $\overline{K}$ clock rising edge. Continuous write operations are initiated with K rising edge. And "early write" data is presented to the device on every rising edge of both K and $\overline{K}$ clocks.When the $\overline{W}$ is disabled, the S7Q163662M and S7Q161862M will enter into deselect mode. The device disregards input data presented on the same cycle $\overline{W}$ disabled.The S7Q163662M and S7Q161862M support byte write operations. With activating $\overline{BW_0}$ or $\overline{BW_1}$ ($\overline{BW_2}$ or $\overline{BW_3}$) in write cycle, only one byte of input data is presented. In S7Q161862M, $\overline{BW_0}$ controls write operation to D0:D8, $\overline{BW_1}$ controls write operation to D9:D17. And in S7Q163662M, $\overline{BW_2}$ controls write operation to D18:D26, $\overline{BW_3}$ controls write operation to D27:D35.

Single Clock Mode

S7Q163662M and S7Q161862M can be operated with the single clock pair K and $\overline{K}$, instead of C or $\overline{C}$ for output clocks. To operate these devices in single clock mode, C and $\overline{C}$ must be tied high during power up and must be maintained high during operation. After power up, this device can't change to or from single clock mode. System flight time and clock skew could not be compensated in this mode.

Depth Expansion

Separate input and output ports enables easy depth expansion. Each port can be selected and deselected independently and read and write operation do not affect each other. Before chip deselected, all read and write pending operations are completed.

Programmable Impedance Output Buffer Operation

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to Vss through a precision resistor (RQ). The value of RQ (within 15%) is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.
To guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

NETSOL

STATE DIAGRAM
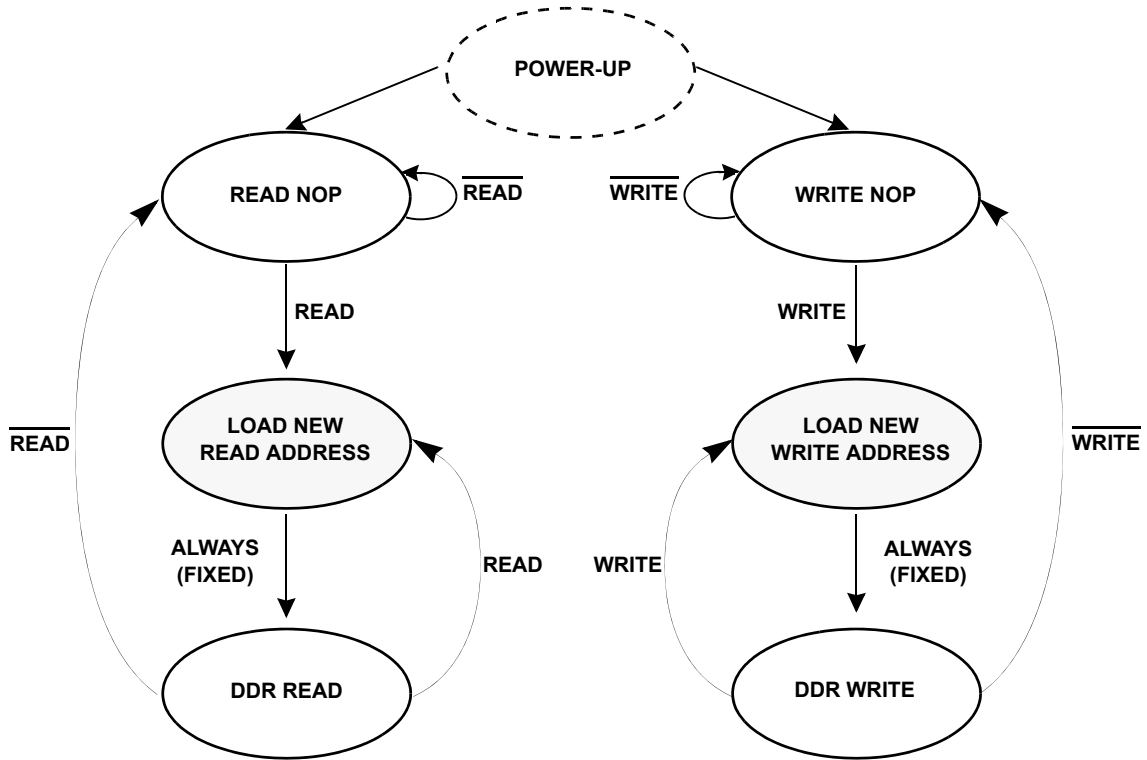
Notes: 1. Internal burst counter is fixed as 2-bit linear, i.e. when first address is A0+0, next internal burst address is A0+1.

2. "READ" refers to read active status with $\overline{R}$=Low, "$\overline{READ}$" refers to read inactive status with $\overline{R}$=high. "WRITE" and "$\overline{WRITE}$" are the same case.

3. Read and write state machine can be active simultaneously.

4. State machine control timing sequence is controlled by K.

Truth Tables

SYNCHRONOUS TRUTH TABLE

K	$\overline{R}$	$\overline{W}$	D		Q		Operation
			D(A0)	D(A1)	Q(A0)	Q(A1)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	High-Z	High-Z	No Operation
↑	L	X	X	X	Dout at C(t+1)	Dout at $\overline{C}$(t+1)	Read
↑	X	L	Din at K(t)	Din at $\overline{K}$(t)	X	X	Write

Notes: 1. X means "Don't Care".

    2. The rising edge of clock is symbolized by (↑).

    3. Before enter into clock stop status, all pending read and write operations will be completed.

WRITE TRUTH TABLE(x18)

K	$\overline{K}$	$\overline{W}$	$\overline{BW_0}$	$\overline{BW_1}$	Operation
↑		H	X	X	READ/NOP
	↑	H	X	X	READ/NOP
↑		L	L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	L	H	WRITE BYTE 0 (K↑)
	↑	L	L	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		L	H	L	WRITE BYTE 1 (K↑)
	↑	L	H	L	WRITE BYTE 1 ($\overline{K}$↑)
↑		L	H	H	WRITE NOTHING (K↑)
	↑	L	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".

    2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).

WRITE TRUTH TABLE(x36)

K	$\overline{K}$	$\overline{W}$	$\overline{BW_0}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	Operation
↑		H	X	X	X	X	READ/NOP
	↑	H	X	X	X	X	READ/NOP
↑		L	L	L	L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	L	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	L	H	H	H	WRITE BYTE 0 (K↑)
	↑	L	L	H	H	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		L	H	L	H	H	WRITE BYTE 1 (K↑)
	↑	L	H	L	H	H	WRITE BYTE 1 ($\overline{K}$↑)
↑		L	H	H	L	L	WRITE BYTE 2 and BYTE 3 (K↑)
	↑	L	H	H	L	L	WRITE BYTE 2 and BYTE 3 ($\overline{K}$↑)
↑		L	H	H	H	H	WRITE NOTHING (K↑)
	↑	L	H	H	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".

    2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).

NETSOL

Absolute Maximum Ratings*

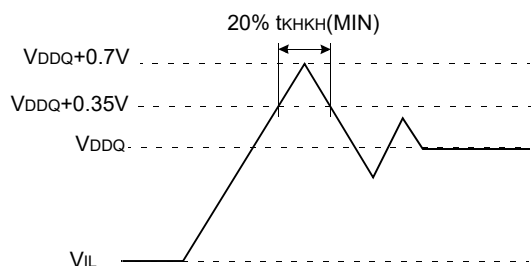| Parameter		Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.5 to 3.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	-0.5 to V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.5 to V_{DD}+0.3	V
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial / Industrial	T_{OPR}	0 to 70 / -40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

*Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

    2. V_{DDQ} must not exceed V_{DD} during normal operation.

DC Electrical Characteristics

Parameter	Symbol	test Conditions		Min	Max	Unit	Notes
Input Leakage Current	I_{IL}	V_{DD}=Max; V_{IN}=V_{SS} to V_{DDQ}		-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	μA	
Operating Current (x36)	I_{CC}	V_{DD}=Max, I_{OUT}=0mA Cycle Time $\geq$ t_{KHKH} Min	-16	-	430	mA	1,5
Operating Current (x18)	I_{CC}	V_{DD}=Max, I_{OUT}=0mA Cycle Time $\geq$ t_{KHKH} Min	-16	-	380	mA	1,5
Standby Current (NOP)	I_{SB1}	Device deselected, I_{OUT}=0mA, f=Max, All Inputs$\leq$0.2V or $\geq$ V_{DD}-0.2V	-16	-	230	mA	1,6
Output High Voltage	V_{OH1}			V_{DDQ}/2	V_{DDQ}	V	2,7
Output Low Voltage	V_{OL1}			V_{SS}	V_{DDQ}/2	V	3,7
Output High Voltage	V_{OH2}	I_{OH}=-1.0mA		V_{DDQ}-0.2	V_{DDQ}	V	4
Output Low Voltage	V_{OL2}	I_{OL}=1.0mA		V_{SS}	0.2	V	4
Input Low Voltage	V_{IL}			-0.3	V_{REF}-0.1	V	8,9
Input High Voltage	V_{IH}			V_{REF}+0.1	V_{DDQ}+0.3	V	8,10

Notes: 1. Minimum cycle. I_{OUT}=0mA.

    2. $|I_{OH}|$=(V_{DDQ}/2)/(RQ/5) for 175Ω $\leq$ RQ $\leq$ 350Ω.

    3. $|I_{OL}|$=(V_{DDQ}/2)/(RQ/5) for 175Ω $\leq$ RQ $\leq$ 350Ω.

    4. Minimum Impedance Mode when ZQ pin is connected to V_{DD}.

    5. Operating current is calculated with 50% read cycles and 50% write cycles.

    6. Standby Current is only after all pending read and write burst operations are completed.

    7. Programmable Impedance Mode.

    8. These are DC test criteria. DC design criteria is V_{REF}±50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.

    9. V_{IL} (Min.) DC=-0.3V, V_{IL} (Min)AC=-1.5V(pulse width $\leq$ 3ns).

    10. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=V_{DDQ}+0.85V(pulse width $\leq$ 3ns).

Overshoot Timing

Undershoot Timing
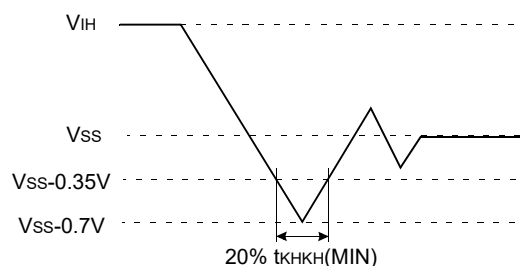
Recommended DC Operating Conditions $(0°C \leq T_A \leq 70°C)$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	1.7	2.5	2.6	V
	V_{DDQ}	1.4	1.5	1.9	V
Reference Voltage	V_{REF}	0.68	0.75	0.95	V
Ground	V_{SS}	0	0	0	V

AC Timing Characteristics

Parameter	Symbol	-16		Unit	Notes
		Min	Max		
Clock					
Clock Cycle Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKH}	6.0		ns	
Clock High Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKL}	2.4		ns	
Clock Low Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KLKH}	2.4		ns	
Clock to $\overline{Clock}$ (K↑ → $\overline{K}$↑, C↑ → $\overline{C}$↑)	$t_{KH\overline{K}H}$	2.7	3.3	ns	
Clock to data clock (K↑ → C↑, $\overline{K}$↑→ $\overline{C}$↑)	t_{KHCH}	0.0	2.0	ns	
Output Times					
C, $\overline{C}$ High to Output Valid	t_{CHQV}		2.5	ns	3
C, $\overline{C}$ High to Output Hold	t_{CHQX}	1.2		ns	3
C, High to Output High-Z	t_{CHQZ}		2.5	ns	3
C, High to Output Low-Z	t_{CHQX1}	1.2		ns	3
Setup Times					
Address valid to K rising edge	t_{AVKH}	0.7		ns	
Control inputs valid to K rising edge	t_{IVKH}	0.7		ns	2
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.7		ns	
Hold Times					
K rising edge to address hold	t_{KHAX}	0.7		ns	
K rising edge to control inputs hold	t_{KHIX}	0.7		ns	
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.7		ns	

Notes: 1. All address inputs must meet the specified setup and hold times for all latching clock edges.
    2. Control singles are $\overline{R}$, $\overline{W}$, $\overline{BW_0}$, $\overline{BW_1}$ and $\overline{BW_2}$, $\overline{BW_3}$, also for x36
    3. If C,$\overline{C}$ are tied high, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
    4. To avoid bus contention, at a given voltage and temperature t_{CHQX1} is bigger than t_{CHQZ}.
    The specs as shown do not imply bus contention because t_{CHQX1} is a MIN parameter that is worst case at totally different test conditions
    (0°C, 2.6V) than t_{CHQZ}, which is a MAX parameter (worst case at 70°C, 2.4V)
   It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

NETSOL

AC Test Conditions

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V_{DD}	1.7~2.6	V
Output Power Supply Voltage	V_{DDQ}	1.4~1.9	V
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V
Input Reference Level	V_{REF}	0.75	V
Input Rise/Fall Time	T_R/T_F	0.3/0.3	ns
Output Timing Reference Level		$V_{DDQ}/2$	V

Note: Parameters are tested with RQ=250Ω

AC Test Output Load
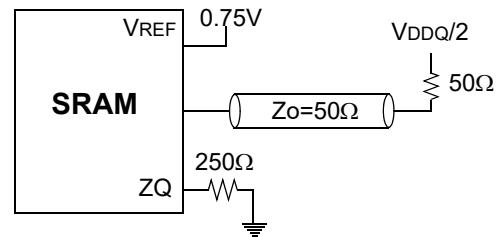
Pin Capacitance

Parameter	Symbol	Test Condition	Typ	Max	Unit	Notes
Address Control Input Capacitance	C_{IN}	V_{IN}=0V	3.5	4	pF	
Input and Output Capacitance	C_{OUT}	V_{OUT}=0V	4	5	pF	
Clock Capacitance	C_{CLK}	-	3	4	pF	

Note: 1. Parameters are tested with RQ=250Ω and V_{DDQ}=1.5V.

2. Periodically sampled and not 100% tested.

Thermal Resistance

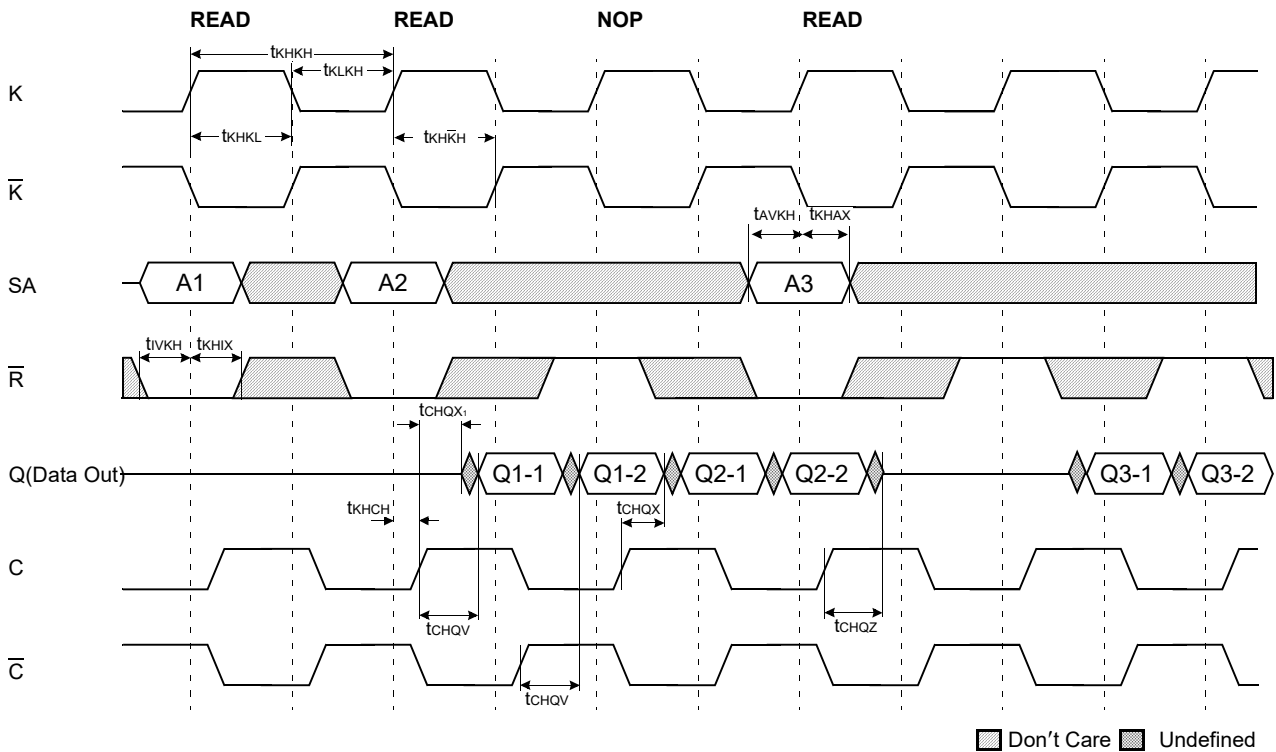| Parameter	Symbol	Typical	Unit	Notes
Junction to Ambient	$θ_{JA}$	16.3	°C/W	
Junction to Case	$θ_{JC}$	2.3	°C/W	
Junction to Pins	$θ_{JB}$	4.3	°C/W	

Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J=T_A + P_D \times θ_{JA}$

Application Information

1Mx18
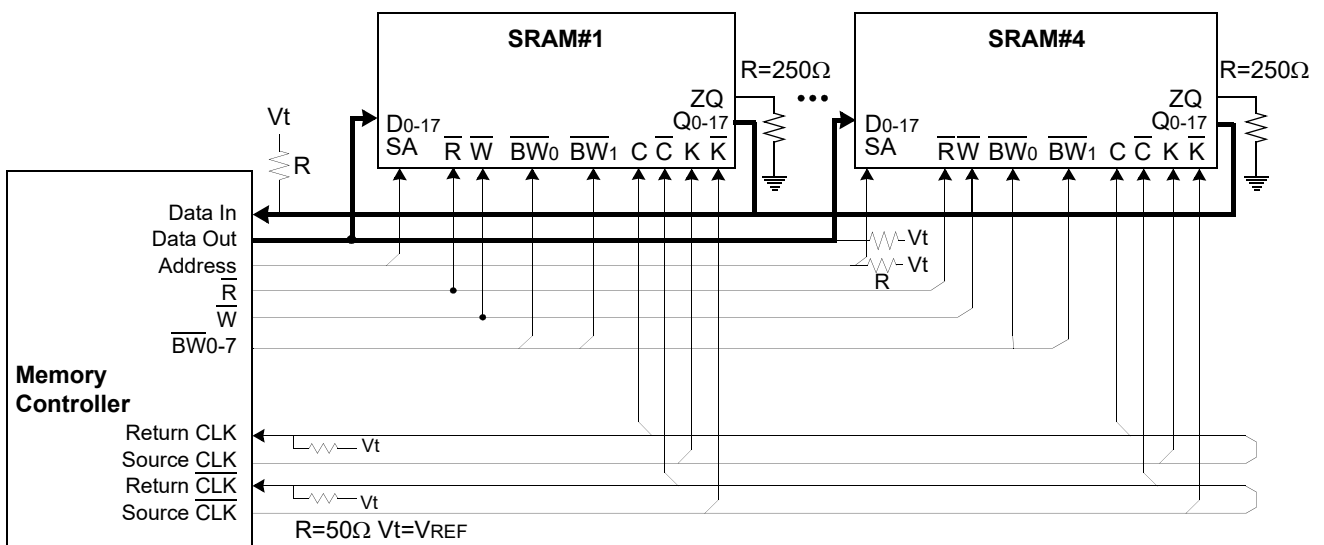
TIMING WAVE FORMS OF READ AND NOP

Note: 1. Q1-1 refers to output from address A1+0, Q1-2 refers to output from address A1+1 i.e. the next internal burst address following A1+0.

2. Outputs are disabled(High-Z) one cycle after a NOP.

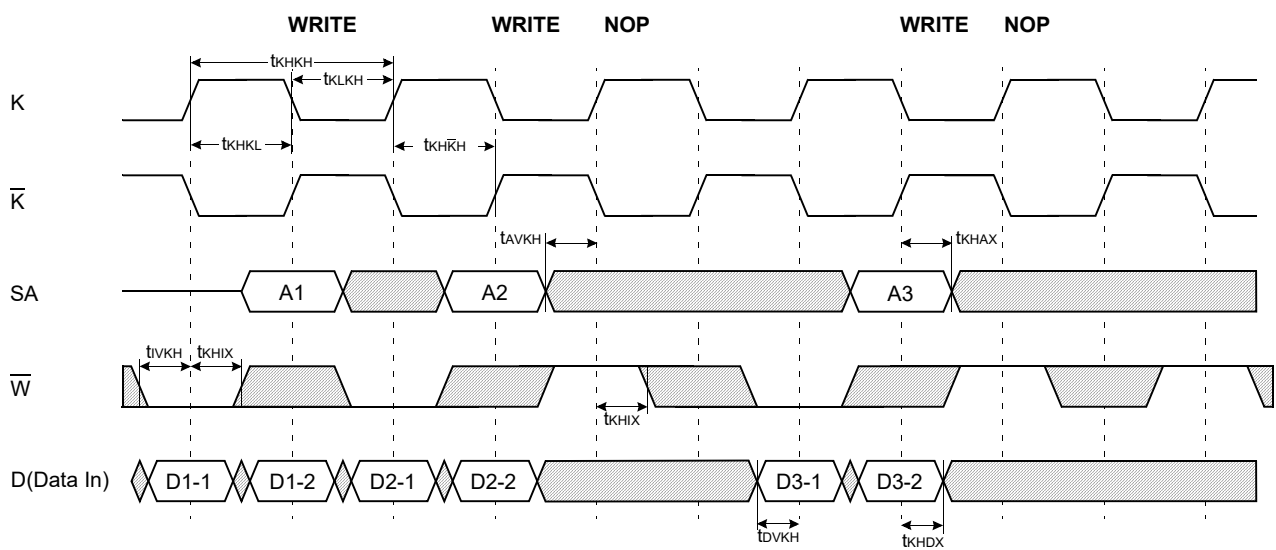## TIMING WAVE FORMS OF WRITE AND NOP
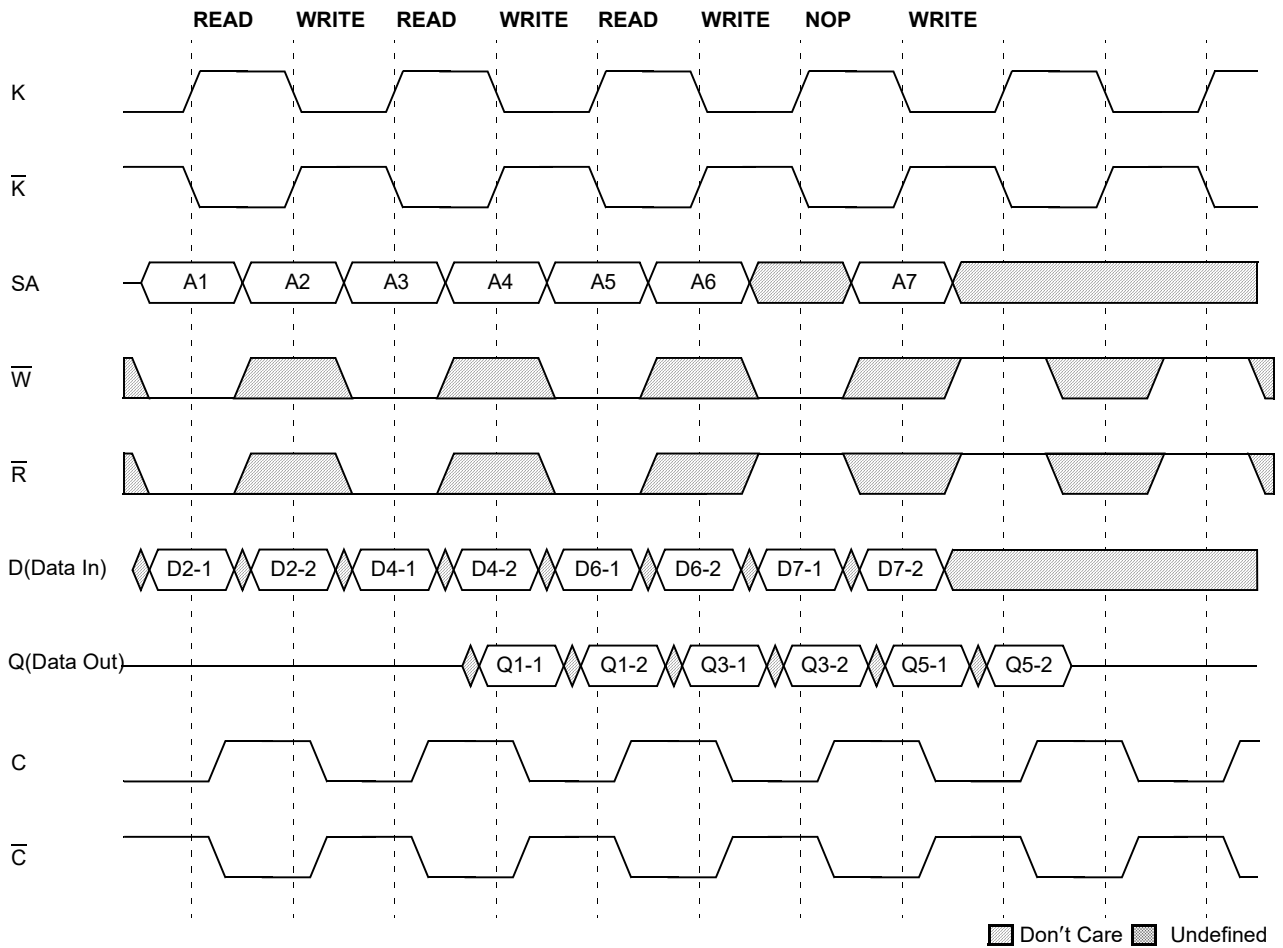
TIMING WAVE FORMS OF READ, WRITE AND NOP

Note: 1. Q1-1 refers to output from address A1+0, Q1-2 refers to output from address A1+1 i.e. the next internal burst address following A1+0.

2. Outputs are disabled(High-Z) one cycle after a NOP.

3. If address A1=A2, data Q1-1=D2-1, data Q1-2=D2-2. Write data is forwarded immediately as read results.

4. $\overline{BW}$x are assumed active.

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP).The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.
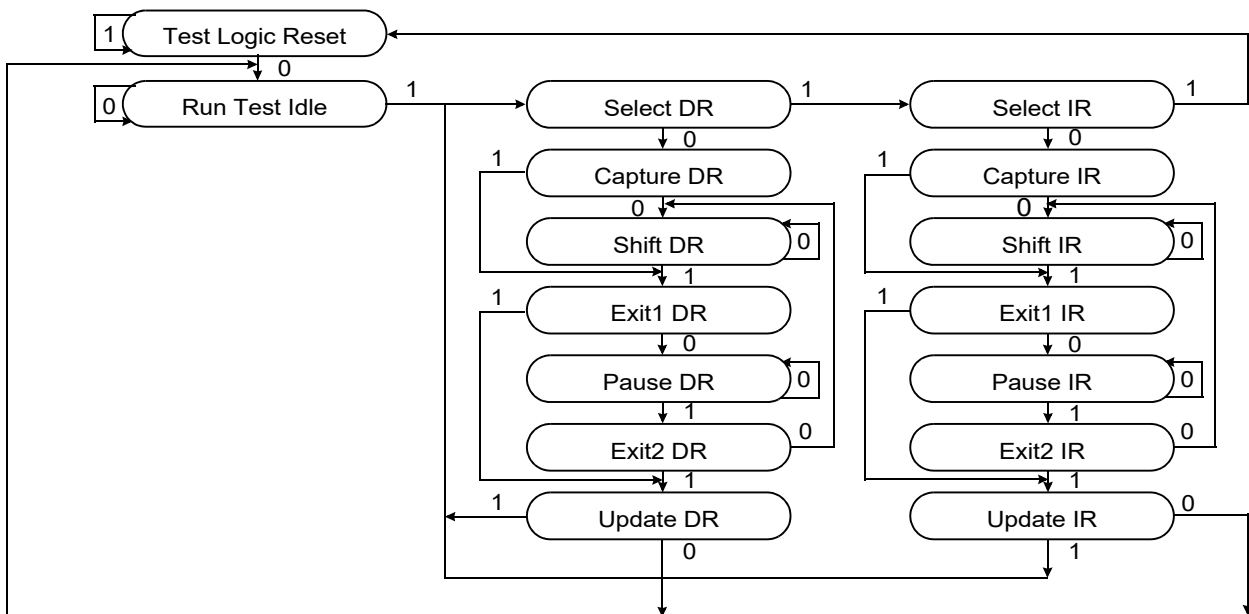
JTAG Block Diagram
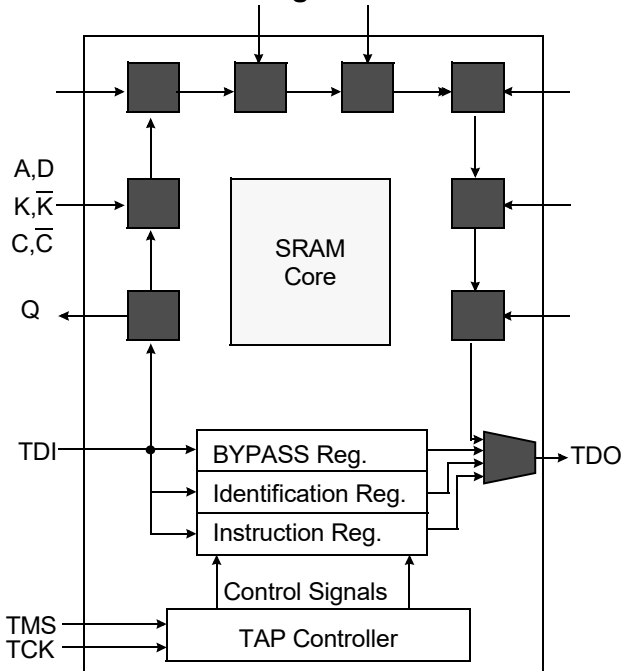
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	RESERVED	Do Not Use	6
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	RESERVED	Do Not Use	6
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.

2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.

3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.

4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.

5. SAMPLE instruction dose not places DQs in Hi-Z.

6. This instruction is reserved for future use.

TAP Controller State Diagram

Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512K x 36 1M x 18	3 bits	1 bit	32 bits	107 bits

ID Registration Definition

Part	Revision Number (31:29)	Part Configuration (28:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
512K x 36 1M x 18	000	00def0wx0t0q0b0s0	01111011001	1

Note: Part Configuration

/def=001 for 18Mb, /wx=11 for x36, 10 for x18

/t=Don't Care., /q=1 for Quadruple, 0 for DDR /b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

Boundary Scan Exit Order

Order	Pin ID	Order	Pin ID	Order	Pin ID
1	6R	37	10D	73	2C
2	6P	38	9E	74	3E
3	6N	39	10C	75	2D
4	7P	40	11D	76	2E
5	7N	41	9C	77	1E
6	7R	42	9D	78	2F
7	8R	43	11B	79	3F
8	8P	44	11C	80	1G
9	9R	45	9B	81	1F
10	11P	46	10B	82	3G
11	10P	47	11A	83	2G
12	10N	48	Internal	84	1J
13	9P	49	9A	85	2J
14	10M	50	8B	86	3K
15	11N	51	7C	87	3J
16	9M	52	6C	88	2K
17	9N	53	8A	89	1K
18	11L	54	7A	90	2L
19	11M	55	7B	91	3L
20	9L	56	6B	92	1M
21	10L	57	6A	93	1L
22	11K	58	5B	94	3N
23	10K	59	5A	95	3M
24	9J	60	4A	96	1N
25	9K	61	5C	97	2M
26	10J	62	4B	98	3P
27	11J	63	3A	99	2N
28	11H	64	1H	100	2P
29	10G	65	1A	101	1P
30	9G	66	2B	102	3R
31	11F	67	3B	103	4R
32	11G	68	1C	104	4P
33	9F	69	1B	105	5P
34	10F	70	3D	106	5N
35	11E	71	3C	107	5R
36	10E	72	1D		

Note: 1. NC pins are read as "X" (i.e. don't care.)

NETSOL

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	2.5	2.6	V	
Input High Level	V_{IH}	$0.7*V_{DD}$	-	$V_{DD}+0.3$	V	
Input Low Level	V_{IL}	-0.3	-	$0.3*V_{DD}$	V	
Output High Voltage (I_{OH}=-2mA)	V_{OH}	$0.75*V_{DD}$	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	$0.25*V_{DD}$	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC Test Conditions

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	V_{DD}/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		V_{DD}/2	V	1

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG Timing Diagram
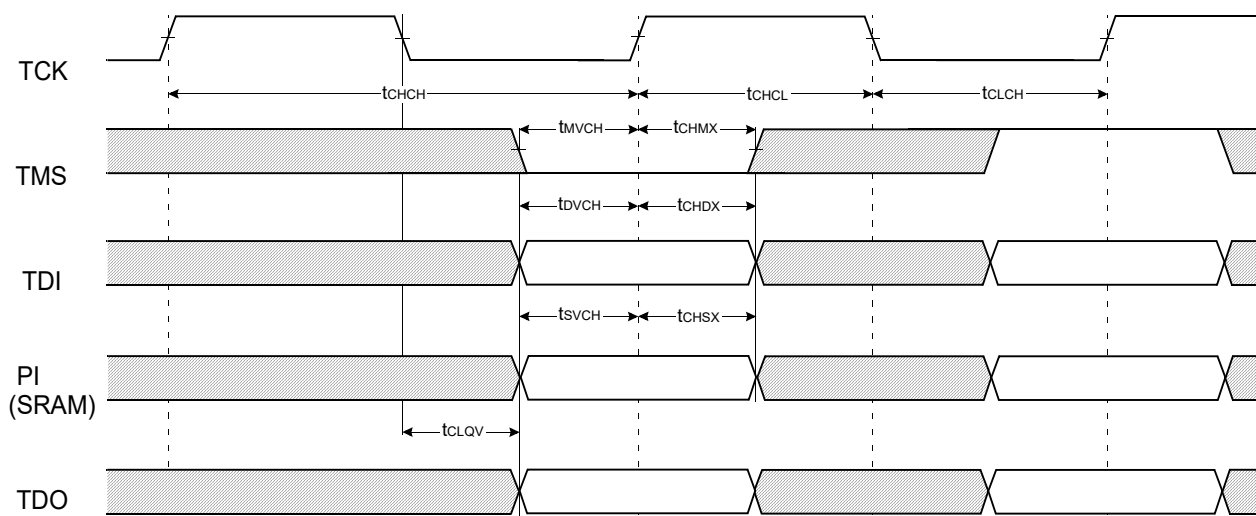
165 FBGA Package Dimensions - Lead & Lead Free
13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array

Top View

Bottom View

Side View
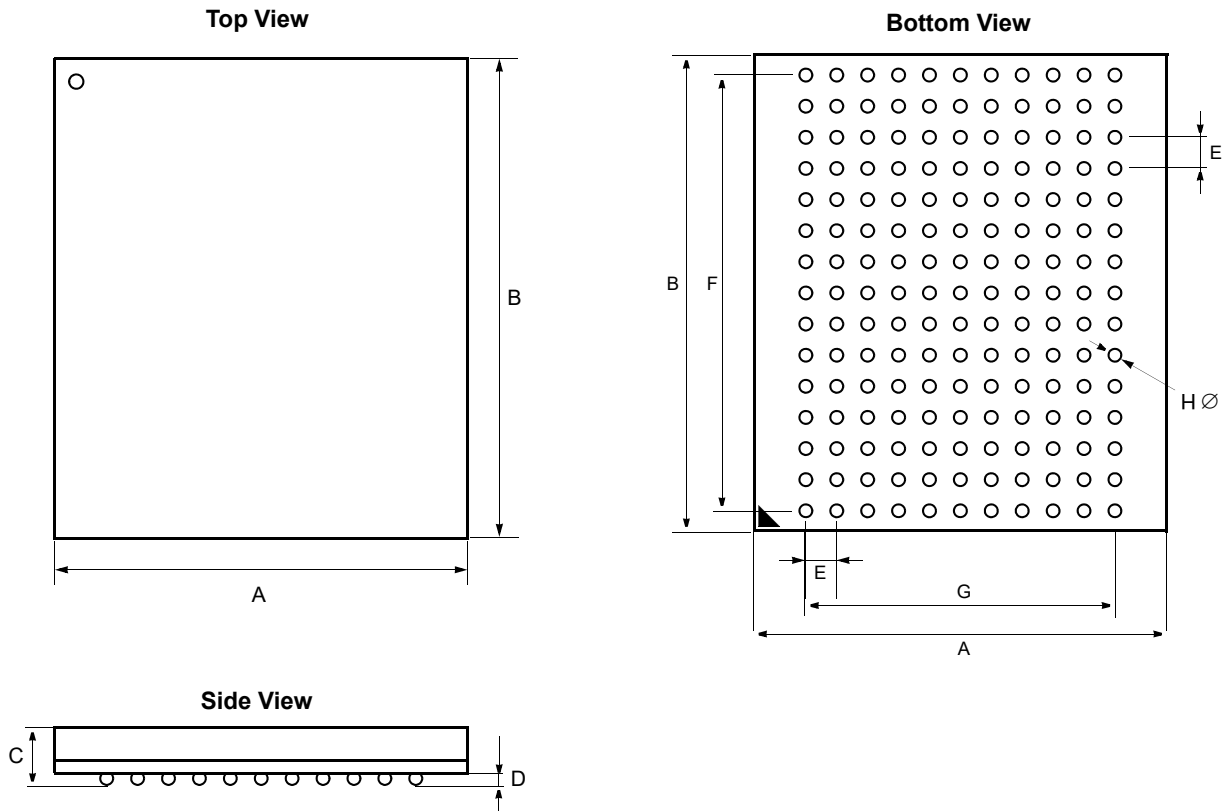
Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		**E**	1.0	mm	
B	15 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	

Rev. 1.1 Apr. 2013

NETSOL