32Mb PPI MRAM M-die

Parallel Peripheral Interface MRAM

3.3V/1.8V

- **S3R3216V1M**
- **S3R3216R1M**

Datasheet

Feature

- Interface
  - Parallel Asynchronous and Page Mode Interface
- Page Mode Read Access
  - Interpage read access : 70ns
  - Intrapage read access : 15ns
- Page Mode Write Access
  - Interpage write access : 320ns
  - Intrapage write access : 15ns
- Page Size
  - x16 I/O Mode : 4-word page size
- Low Power Consumption
  - Read current(3.3V) : 14mA
  - Write current(3.3V) : 16mA
  - Read current(1.8V) : 10mA
  - Write current(1.8V) : 15mA
  - Standby current(3.3V) : 700uA
  - Standby current(1.8V) : 600uA
- Data Byte Control(x16 I/O Mode)
  - $\overline{LB}$: DQ_7~DQ_0, $\overline{UB}$: DQ_{15}~DQ_8
- Memory cell : STT-MRAM
  - nonvolatile
- Density
  - 32Mb
- Data Integrity : No external ECC required
- Data Endurance
  - Unlimited read cycle
  - 10^{14} write cycles
- Data Retention
  - 10 years at 85°C
- Single Power Supply Operation
  - S3R3216V1M: 2.70V~3.60V
  - S3R3216R1M: 1.71V~1.98V
- Operating Temperature Range
  - Industrial Temperature : -40°C to 85°C
- RoHS compliant packages
  - 48FBGA (6 ㎜ x 8 ㎜)
  - 54TSOP2 (10 ㎜ x 22 ㎜)

Performance

Operation	Symbol	Typical Values		Units
		1.8V (S3R3216R1M)	3.3V (S3R3216V1M)	
Interpage Read Cycle Time	t_{RC}	70(Min.)		ns
Intrapage Read Cycle Time	t_{PRC}	15(Min.)		ns
Interpage Write Cycle Time	t_{WC}	320(Min.)		ns
Intrapage Write Cycle Time	t_{PWC}	15(Min.)		ns
Standby Current	I_{SB}	600	700	uA
Interpage Read Current	I_{CCR}	10	14	mA
Intrapage Read Current	I_{CCRP}	10	14	mA
Interpage Write Current	I_{CCW}	15	16	mA
Intrapage Write Current	I_{CCWP}	15	16	mA

Table of Contents

General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM).
Data is always non-volatile and the device can replace FRAM, low-power SRAM or nvSRAM with same functionality and help to simplify system design. Due to the non-volatility and virtually unlimited endurance characteristics of STT-MRAM, it is suited for code storage, data logging, backup memory and working memory in industrial designs.

It is a fully random-access memory with parallel asynchronous interface. And x16 I/O mode allows that lower and upper byte access by data byte control ($\overline{LB}$, $\overline{UB}$).
It supports the asynchronous page mode function to enhance the read and write performance. The page size is 4 words.

The S3R3216(V/R)1M is packaged in industrial standard 54TSOP2 and 48FBGA. These packages are compatible with similar low-power volatile and non-volatile products.
The device is offered with industrial (-40°C to 85°C) operating temperature range.

Pin Description – 3.3V Device

Figure 1 : Functional Block Diagram – 3.3V Device

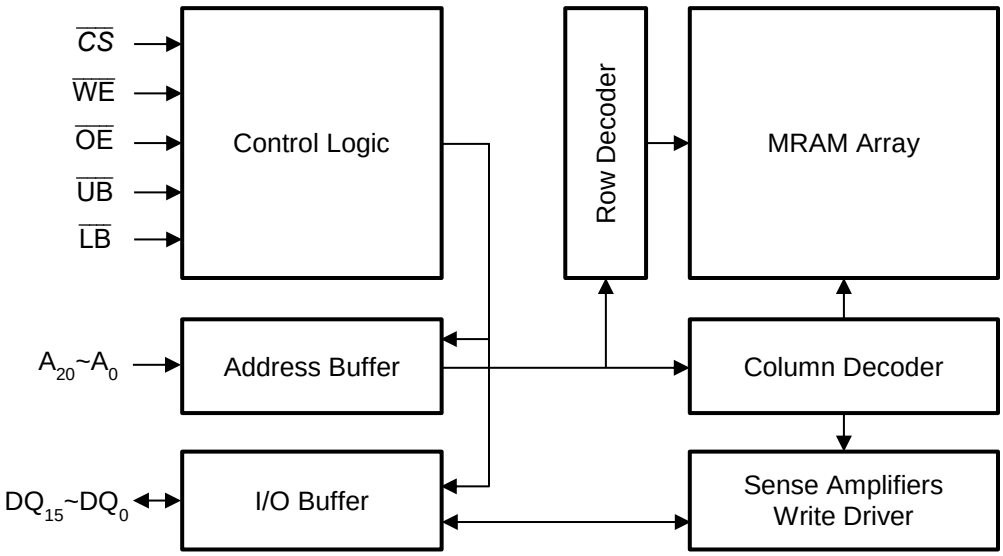


Table 1 : Pin Description – 3.3V Device

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select**: When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
$\overline{WE}$	Input	**Write Enable**: When $\overline{CS}$ and $\overline{WE}$ are driven Low, write operation is initiated. The rising edge of $\overline{CS}$ causes the device to transfer the data to memory array. The rising edge of $\overline{WE}$ latches the input data. And, the falling edge of $\overline{WE}$ latches a new page address for write cycles.
$\overline{OE}$	Input	**Output Enable**
$\overline{LB}$	Input	**Lower Byte Control**: DQ_7~DQ_0
$\overline{UB}$	Input	**Upper Byte Control**: DQ_{15}~DQ_8
A_{20}~A_0	Input	**Address** The LSB address A_1~A_0 are used for page mode read and write operation.
DQ_{15}~DQ_0	Bidirectional	**Data Input/Outputs**
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use : DNUs must be left unconnected.

Pin Description – 1.8V Device

Figure 2 : Functional Block Diagram – 1.8V Device

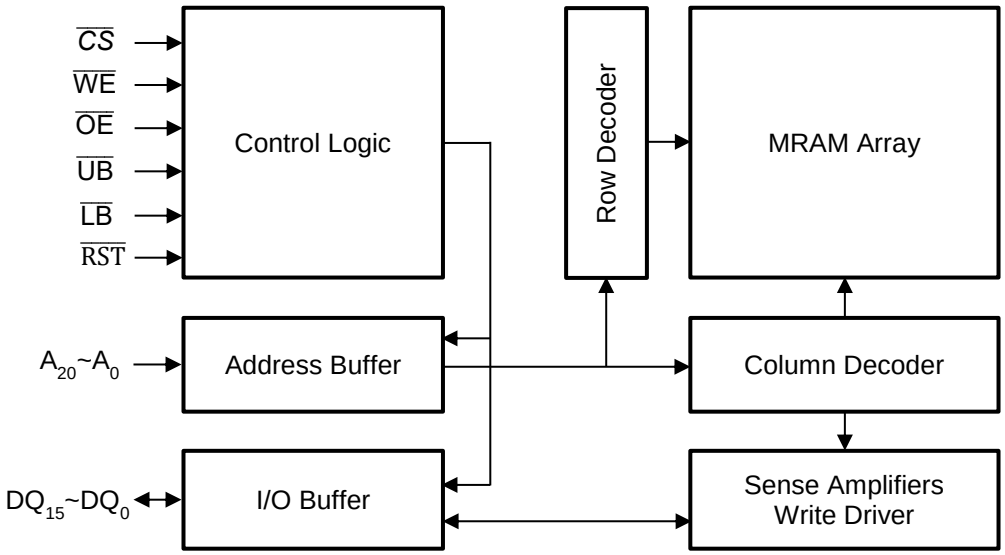
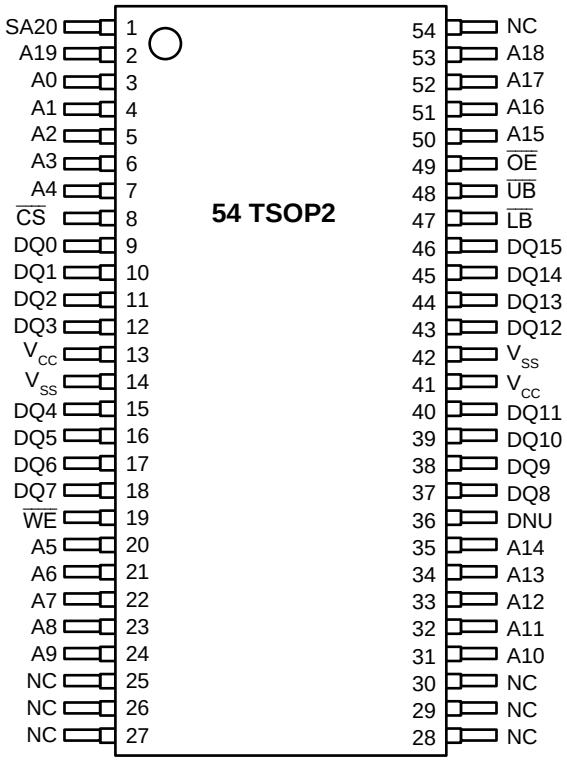


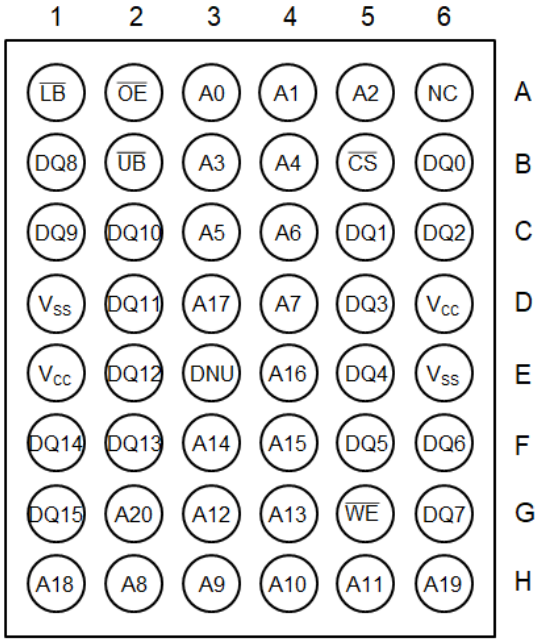
Table 2 : Pin Description – 1.8V Device

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select**: When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
$\overline{WE}$	Input	**Write Enable**: When $\overline{CS}$ and $\overline{WE}$ are driven Low, write operation is initiated. The rising edge of $\overline{CS}$ causes the device to transfer the data to memory array. The rising edge of $\overline{WE}$ latches the input data. And, the falling edge of $\overline{WE}$ latches a new page address for write cycles.
$\overline{OE}$	Input	**Output Enable**
$\overline{LB}$	Input	**Lower Byte Control**: DQ_7~DQ_0
$\overline{UB}$	Input	**Upper Byte Control**: DQ_{15}~DQ_8
A_{20}~A_0	Input	**Address** The LSB address A_1~A_0 are used for page mode read and write operation.
DQ_{15}~DQ_0	Bidirectional	**Data Input/Outputs**
$\overline{RST}$	Input	**Reset** $\overline{RST}$ pin is a hardware RESET signal. When $\overline{RST}$ is driven High, the device is in the normal operation mode. When $\overline{RST}$ is driven Low, the device enters in the initialization mode. This pin has an internal pullup resistor.
Vcc	Supply	Power pin
Vss	Supply	Ground pin
NC	-	Not Connected
DNU	-	Do Not Use : DNUs must be left unconnected.

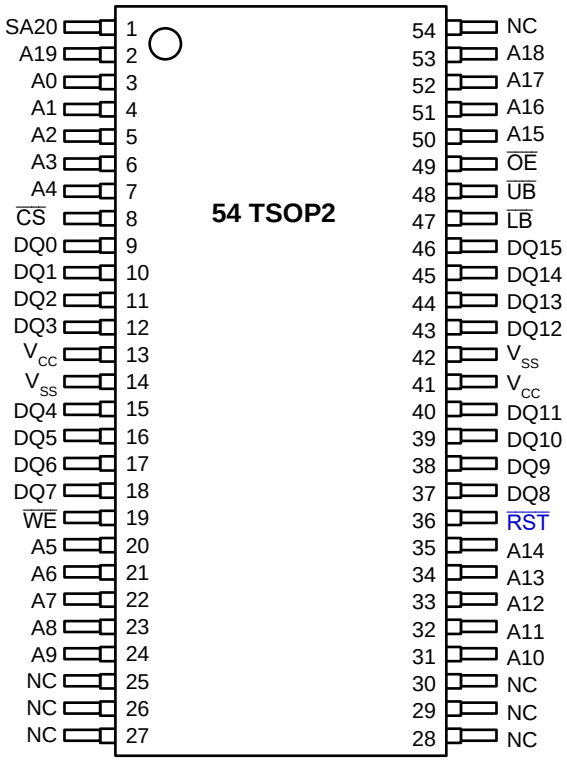
Package Pin Configuration – 3.3V Device



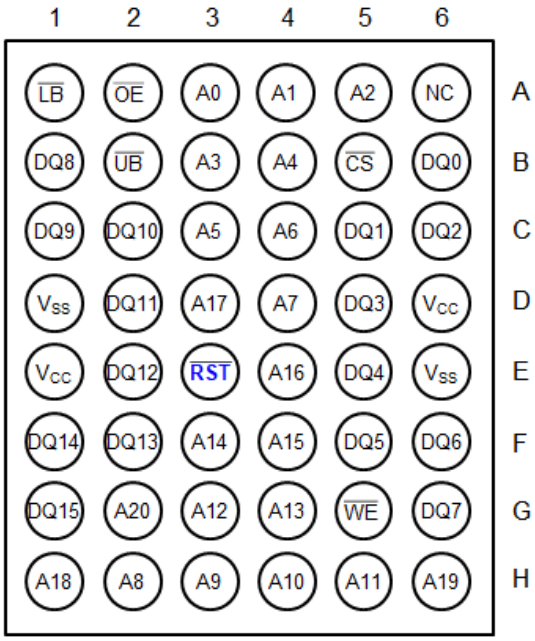
48 Ball FBGA (x16)



Package Pin Configuration – 1.8V Device



48 Ball FBGA (x16)



Functional Description

Functional Description – x16 I/O Mode

Table 3 : Functional Description - x16 I/O mode

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ_7~DQ_0	DQ_{15}~DQ_8	Modes	Supply Current
H	X	X	X	X	High-Z	High-Z	Not Selected	I_{SB}
L	H	H	X	X	High-Z	High-Z	Output disable	I_{CCR}
L	H	L	H	H	High-Z	High-Z	Output disable	I_{CCR}
L	H	L	L	H	Dout	High-Z	Lower Byte Read	I_{CCR}
L	H	L	H	L	High-Z	Dout	Upper Byte Read	I_{CCR}
L	H	L	L	L	Dout	Dout	Word Read	I_{CCR}
L	L	X	H	H	High-Z	High-Z	Input disable	I_{CCW}
L	L	X	L	H	Din	High-Z	Lower Byte Write	I_{CCW}
L	L	X	H	L	High-Z	Din	Upper Byte Write	I_{CCW}
L	L	X	L	L	Din	Din	Word Write	I_{CCW}

Address Pin

Table 4 : Address Pin

Density	Address Pin	Page Address Pin
32Mb	A_{20}~A_0	A_1~A_0

Electrical Specifications

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 5 : Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage on Vcc Supply Relative to VSS: 3.3V Device	-0.5	3.8	V
Voltage on Any Pin relative to VSS : 3.3V Device	-0.5	3.8	V
Voltage on Vcc Supply Relative to VSS: 1.8V Device	-0.5	2.35	V
Voltage on Any Pin relative to VSS : 1.8V Device	-0.5	2.35	V
Storage Temperature	-55	150	°C
Operating Ambient Temperature	-40	85	°C
ESD HBM (Human Body Model)	≥ |2000 V|		V
ESD CDM (Charged Device Model)	≥ |500 V|		V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles - Peak temperature ≤ 260°C - The time above 255°C ≤ 30 seconds - Reflow cycles ≤ 3 times		

Endurance, Retention and Magnetic Immunity

Table 6 : Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Units
Write Endurance	-25°C	10^{14}	-	Cycles/page
Data Retention	85°C	10	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

Recommended Operating Conditions

Table 7 : Recommended Operating Conditions

Parameter / Condition	Min.	Typ.	Max.	Units
Operating Temperature	-40	25	85	°C
Vcc Supply Voltage : 3.3V Device	2.7	3.3	3.6	V
Vcc Supply Voltage : 1.8V Device	1.71	1.8	1.98	V
Vss Supply Voltage	0.0	0.0	0.0	V

Pin Capacitance

Table 8 : Pin Capacitance

Parameter	Conditions	Typ.	Max.	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	-	4	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; $V_{I/O}$ = 0V	-	6	pF

* Capacitance is sampled and not 100% tested

AC Test Condition

Table 9 : AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	1ns/1V
Input and output measurement timing levels	Vcc/2
Output Load	CL = 30pF

DC Characteristics

Table 10 : DC Characteristics : 3.3V Device

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current		I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}	-2	-	+2	uA
Output Leakage Current		I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}	-2	-	+2	uA
Read Current	Random	I_{CCR}	V_{CC} (max), I_{OUT}=0mA	-	14	18	mA
	Page mode	I_{CCRP}	V_{CC} (max), I_{OUT}=0mA	-	14	18	mA
Write Current	Random	I_{CCW}	V_{CC} (max)	-	16	20	mA
	Page mode	I_{CCWP}	V_{CC} (max)	-	16	20	mA
Standby Current		I_{SB}	V_{CC} (max), $\overline{CS} \geq V_{CC}$-0.2V	-	700	950	uA
Input High Voltage		V_{IH}	-	0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xV_{CC}	V
Output High Voltage		V_{OH}	I_{OH}=-1mA	2.4	-	-	V
Output Low Voltage		V_{OL}	I_{OL}=2mA	-	-	0.4	V

Table 11 : DC Characteristics : 1.8V Device

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current		I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}	-2	-	+2	uA
Output Leakage Current		I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}	-2	-	+2	uA
Read Current	Random	I_{CCR}	V_{CC} (max), I_{OUT}=0mA	-	10	14	mA
	Page mode	I_{CCRP}	V_{CC} (max), I_{OUT}=0mA	-	10	14	mA
Write Current	Random	I_{CCW}	V_{CC} (max)	-	15	19	mA
	Page mode	I_{CCWP}	V_{CC} (max)	-	15	19	mA
Standby Current		I_{SB}	V_{CC} (max), $\overline{CS} \geq V_{CC}$-0.2V	-	600	900	uA
Input High Voltage		V_{IH}	-	0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.3xV_{CC}	V
Output High Voltage		V_{OH}	I_{OH}=-1mA	1.4	-	-	V
Output Low Voltage		V_{OL}	I_{OL}=2mA	-	-	0.4	V

AC Timing Parameters

Table 12 : Read AC Timing Parameter

Parameter	Symbol	Min.	Max.	Units
Read Cycle Time (Interpage)	t_{RC}	70	-	ns
Page Read Cycle Time (Intrapage)	t_{PRC}	15	-	ns
$\overline{CS}$ Read Active Time	t_{RCA}	65	-	ns
$\overline{CS}$ Falling to Valid Output Time	t_{CO}	-	65	ns
Address Access Time [2])	t_{AA}	-	80	ns
Page Address Access Time	t_{PAA}	-	15	ns
$\overline{CS}$ Rising to Output Hold Time	t_{COH}	3	-	ns
Address change to Output Hold Time [2])	t_{OH}	30	-	ns
Page address change to Output Hold Time	t_{POH}	5	-	ns
$\overline{OE}$ Falling to Valid Output Time	t_{OE}	-	15	ns
$\overline{UB}$, $\overline{LB}$ Falling to Valid Output Time [1])	t_{BA}	-	15	ns
$\overline{CS}$ Rising to High-Z Output Time	t_{CHZ}	-	8	ns
$\overline{OE}$ Rising to High-Z Output Time	t_{OHZ}	-	8	ns
$\overline{UB}$, $\overline{LB}$ Rising to High-Z Output Time [1])	t_{BHZ}	-	8	ns
Address Transition to $\overline{CS}$ falling Time [2])	t_{CAS}	0	-	ns
$\overline{CS}$ Rising to Address Transition Time [2])	t_{CAH}	0	-	ns
$\overline{WE}$ Rising to $\overline{CS}$ Falling Time	t_{WES}	0	-	ns
$\overline{CS}$ Rising to $\overline{WE}$ Falling Time	t_{WEH}	0	-	ns
$\overline{CS}$ High Time for Read End	t_{CSDR}	5	-	ns
Address Transition Interval Time	t_{AX}	-	5	ns

Notes:
1. Those parameters are applied for x16 I/O mode only.
2. Address except for page address

AC Timing Parameters

Table 13 : Write AC Timing Parameter

Parameters	Symbol	Min	Max	Unit
Write Cycle Time (Interpage)	t_{WC}	320	-	ns
$\overline{CS}$ Write Active Time [3]	t_{WCA}	20	-	ns
$\overline{CS}$ Falling to End of Write Time	t_{CW}	20	-	ns
Page Write Cycle Time (Intrapage)	t_{PWC}	15	-	ns
$\overline{WE}$ Falling to End of Write (invalid output does not appear)	t_{WP}	10	-	ns
$\overline{WE}$ Falling to End of Write (invalid output appears)	t_{WP1}	20	-	ns
$\overline{UB}$, $\overline{LB}$ Falling to End of Write Time [1]	t_{BW}	10	-	ns
$\overline{WE}$ Falling to Output High-Z Time	t_{WHZ}	-	8	ns
Valid Input Data to End of Write Time	t_{DS}	8	-	ns
End of Write to Vaild Input Data Time	t_{DH}	0	-	ns
Address Transition Time to $\overline{CS}$ falling [2]	t_{CAS}	0	-	ns
$\overline{CS}$ Rising to Address Transition Time [2]	t_{CAH}	0	-	ns
Page Address Transition to $\overline{WE}$ falling Time	t_{PAS}	0	-	ns
$\overline{WE}$ falling to Page Address Transition Time	t_{PAH}	10	-	ns
$\overline{WE}$ High Time for Page Write	t_{PWH}	3	-	ns
$\overline{CS}$ High Time for Write End [3]	t_{CSDW}	250	-	ns

Notes:
1. Those parameters are applied for x16 I/O mode only.
2. Address except for page address
3. $t_{WCA} + t_{CSDW} \geq t_{WC}$

Power On/Off Sequence : 3.3V Device

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Normal operation must start after t_{PU}.

Figure 3 : Power-Up/Down Behavior

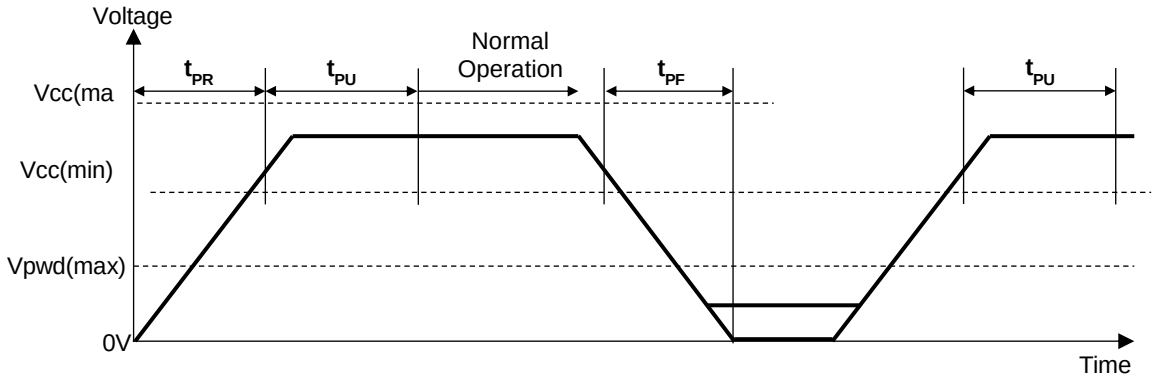


Table 14 : Power-Up/Down Timing

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	2.7	3.6	V
Vcc rising time	t_{PR} (1)	30	-	µs/V
Vcc falling time	t_{PF} (1)	30	-	µs/V
Vcc(min) to $\overline{CS}$ Low (first instruction) time	t_{PU} (1)	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	V_{PWD} (1)	-	1.6	V

Notes:
1: These parameters are guaranteed by characterization; not tested in production.

Power On/Off Sequence : 1.8V Device

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Normal operation must start after t_{PU}.
- Normal operation must start after t_{RST}.

Figure 4 : Power-Up/Down Behavior

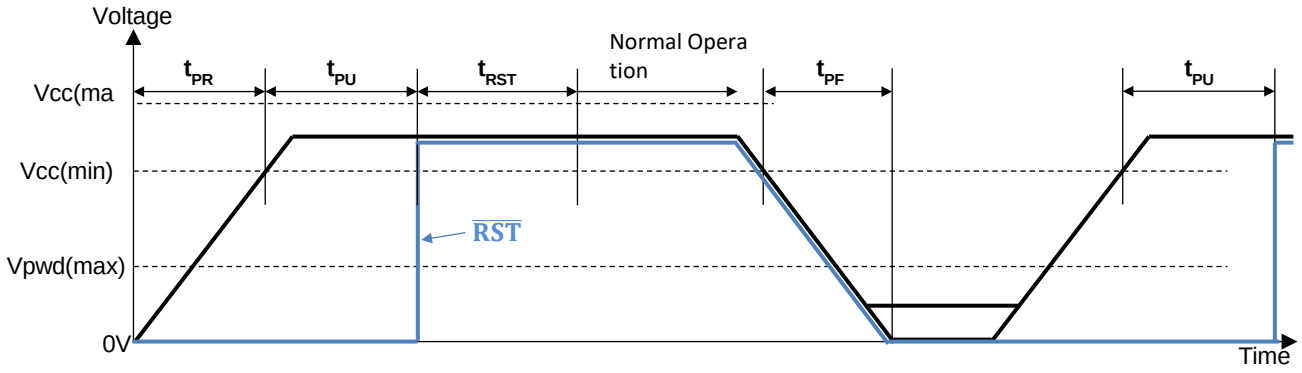


Table 15 : Power-Up/Down Timing

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	1.71	1.98	V
Vcc rising time	t_{PR} (1)	30	-	µs/V
Vcc falling time	t_{PF} (1)	30	-	µs/V
Vcc(min) to $\overline{RST}$ Low time	t_{PU} (1)	1.0	-	ms
$\overline{RST}$ High to $\overline{CS}$ Low (first instruction) time	t_{RST} (1)	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	V_{PWD} (1)	-	0.8	V
Reset Time	t_{RST} (1)	2.0	-	ms

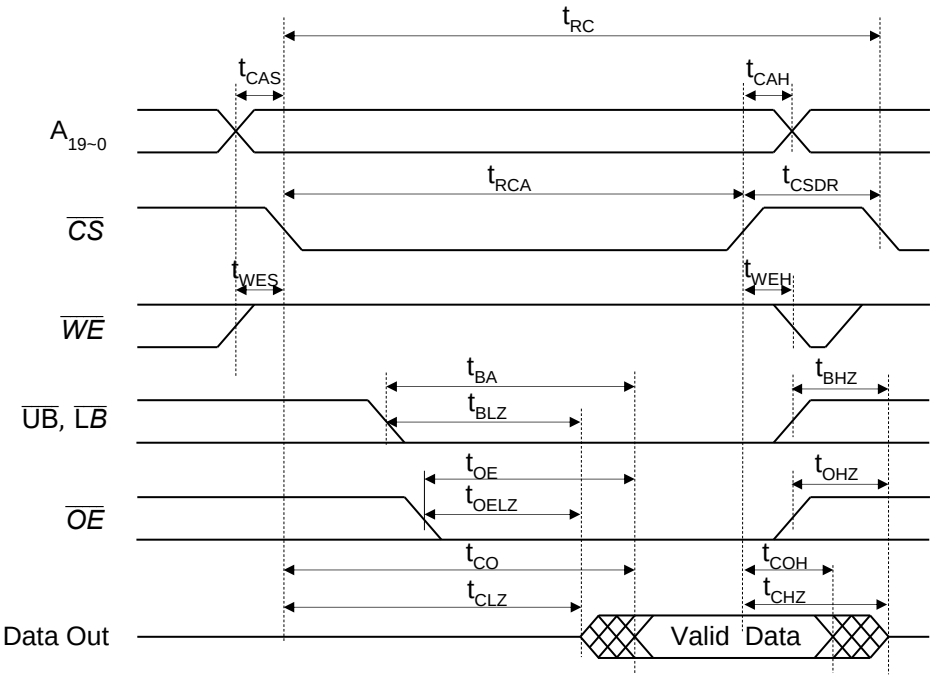
Notes:
1: These parameters are guaranteed by characterization; not tested in production.

Device Operation

Read Operation : Interpage

Read operation is initiated when $\overline{CS}$ goes to low and $\overline{WE}$ is high. The falling edge of $\overline{CS}$ latches the address and starts to read data from memory array. The output data are available after t_{CO} . The minimum random read cycle time is t_{RC}. The data remains in High-Z until the valid data is output.

Figure 5 : Timing Waveform of Read Cycle : x16 I/O mode

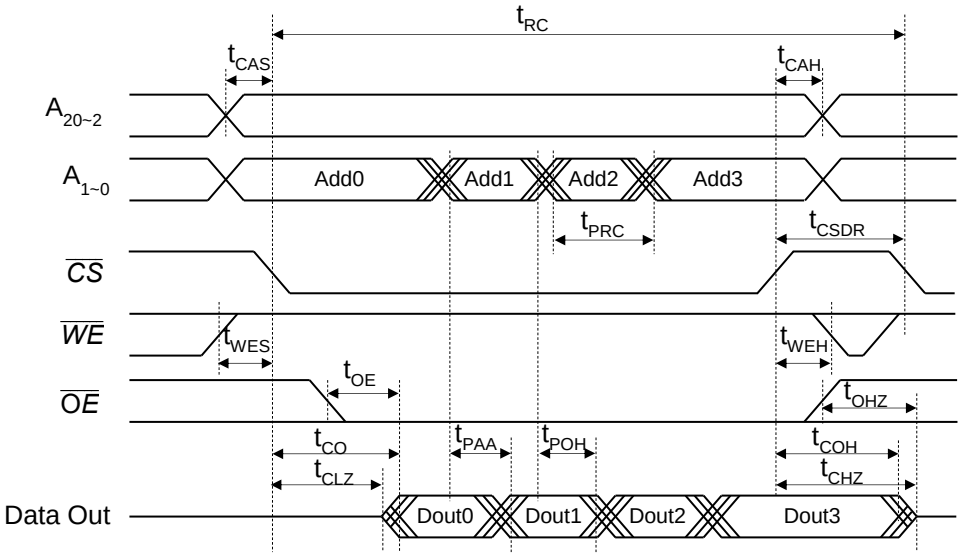


Page Mode Read Operation : Intrapage

The device supports the page mode read function to enhance the read performance. It reads a page data from memory array and latches the data into an internal page buffer.
The first data is output after t_{CO}. When the next page address is input, subsequent data is output from the page buffer after t_{PAA}.
The sequence and length of page address are not restricted.
For example, the sequence A2-A0-A1 is available.

Parameter	x16 I/O mode
Page Address	A_1~A_0
Page size	4-word (8-bytes)

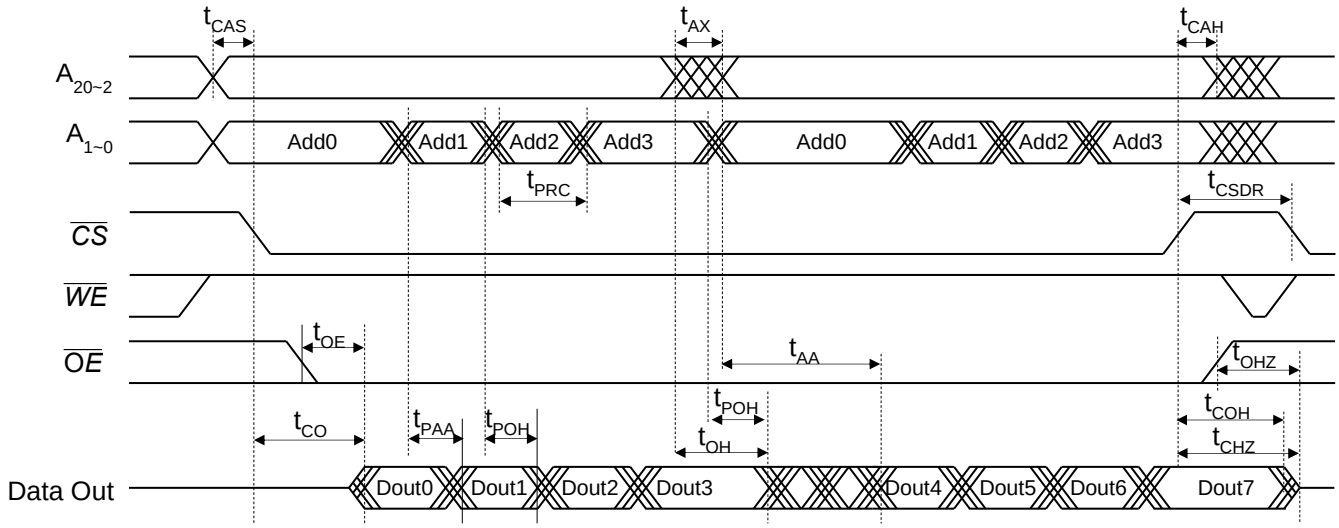
Figure 6 : Timing Waveform of Page Mode Read Cycle : x16 I/O mode



Address Access Read Operation

During $\overline{CS}$ is low and $\overline{WE}$ is high, if a random address (except for the page address) are changed, the device reads a page data from memory array of a new address and latches the data into an internal page buffer. The first data is output after t_{AA}. When the next page address is input, subsequent data is output from the page buffer after t_{PAA}. The random address transition time should not exceed t_{AX}.

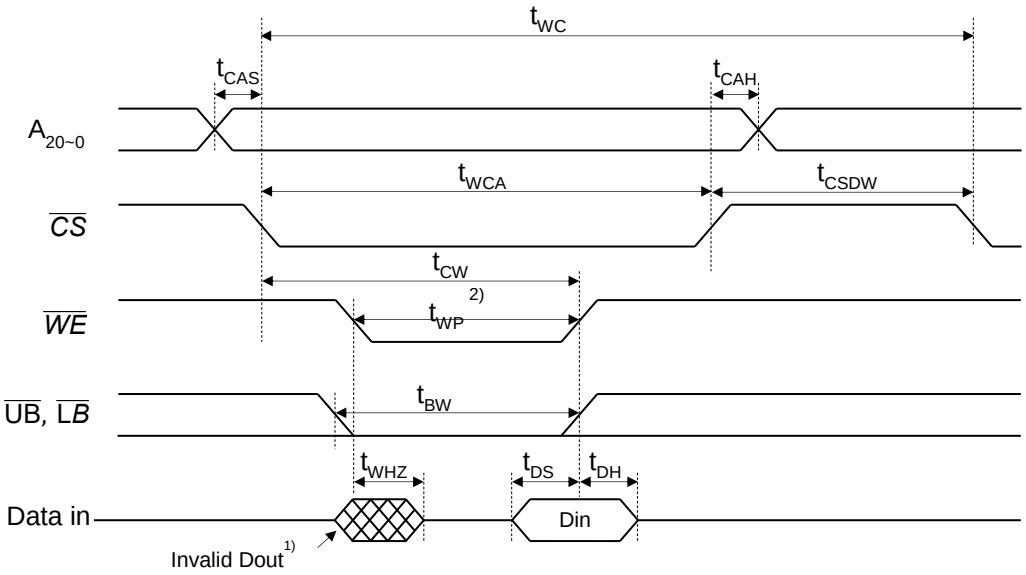
Figure 7 : Timing Waveform of Address Access Read Cycle : x16 I/O mode



Write Operation ($\overline{WE}$ control) : Interpage

Write operation is initiated when $\overline{WE}$ goes to low and $\overline{CS}$ is low. The device latches address on the falling edge of $\overline{CS}$. It latches the lower byte data on the rising edge of $\overline{WE}$ or $\overline{LB}$ and the upper byte data on the rising edge of $\overline{WE}$ or $\overline{UB}$ for x16 I/O mode.
The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array.

Figure 8 : Timing Waveform of Write Cycle ($\overline{WE}$ control) : x16 I/O mode



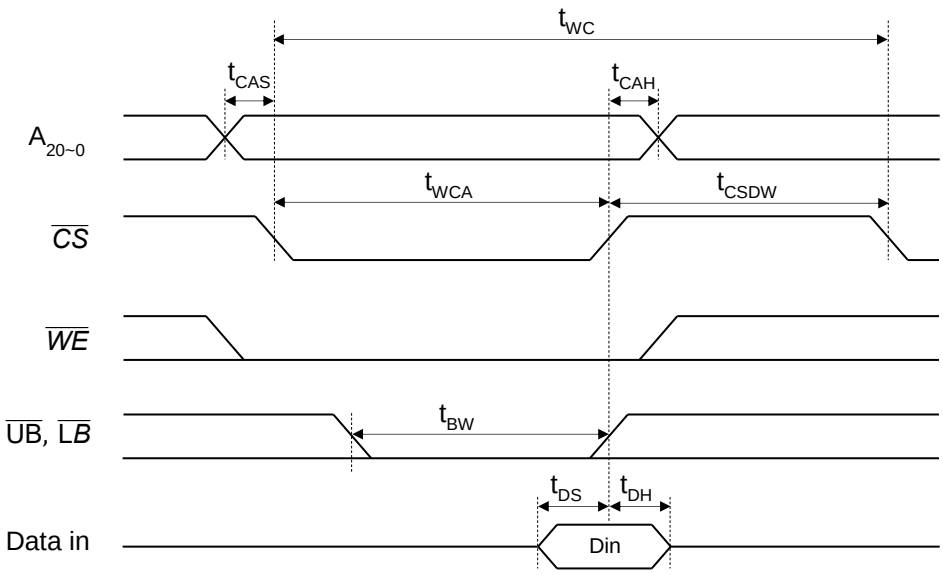
Notes :

1. The data pins remain in High-Z state if the time of $\overline{CS}$ falling to $\overline{WE}$ falling is smaller than 30ns or $\overline{OE}$ is High.
2. In case that the data pins do not remains in High-Z state, t_{WP} should be t_{WP1}
3. $t_{WCA} + t_{CSDW} \geq t_{WC}$

Write Operation ($\overline{CS}$ control) : Interpage

Write operation is initiated when $\overline{CS}$ goes to low and $\overline{WE}$ is low. The device latches address on the falling edge of $\overline{CS}$. It latches the lower byte data on the rising edge of $\overline{CS}$ or $\overline{LB}$ and the upper byte data on the rising edge of $\overline{CS}$ or $\overline{UB}$ for x16 I/O mode.
The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array.

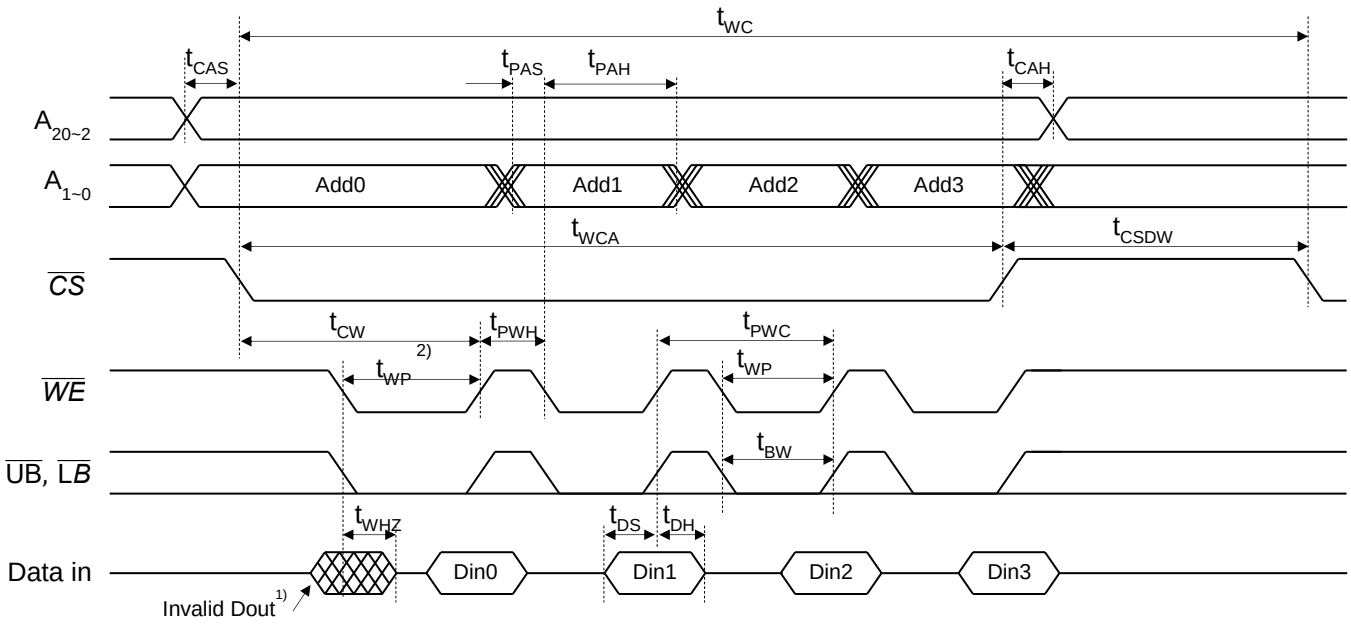
Figure 9 : Timing Waveform of Write Cycle ($\overline{CS}$ control) : x16 I/O mode



Page Mode Write Operation : Intrapage

The device supports the page mode write function to enhance the write performance. It latches a page address every falling edge of $\overline{WE}$.
It latches the lower byte data on every rising edge of $\overline{WE}$ or $\overline{LB}$ and the upper byte data on every rising edge of $\overline{WE}$ or $\overline{UB}$ for x16 I/O mode.
The rising edge of $\overline{CS}$ causes the device to transfer the input data to memory array.
The sequence and length of page address are not restricted. For example, the sequence A2-A0-A1 is available.

Figure 10 : Timing Waveform of Page Mode Write Cycle : x16 I/O Mode



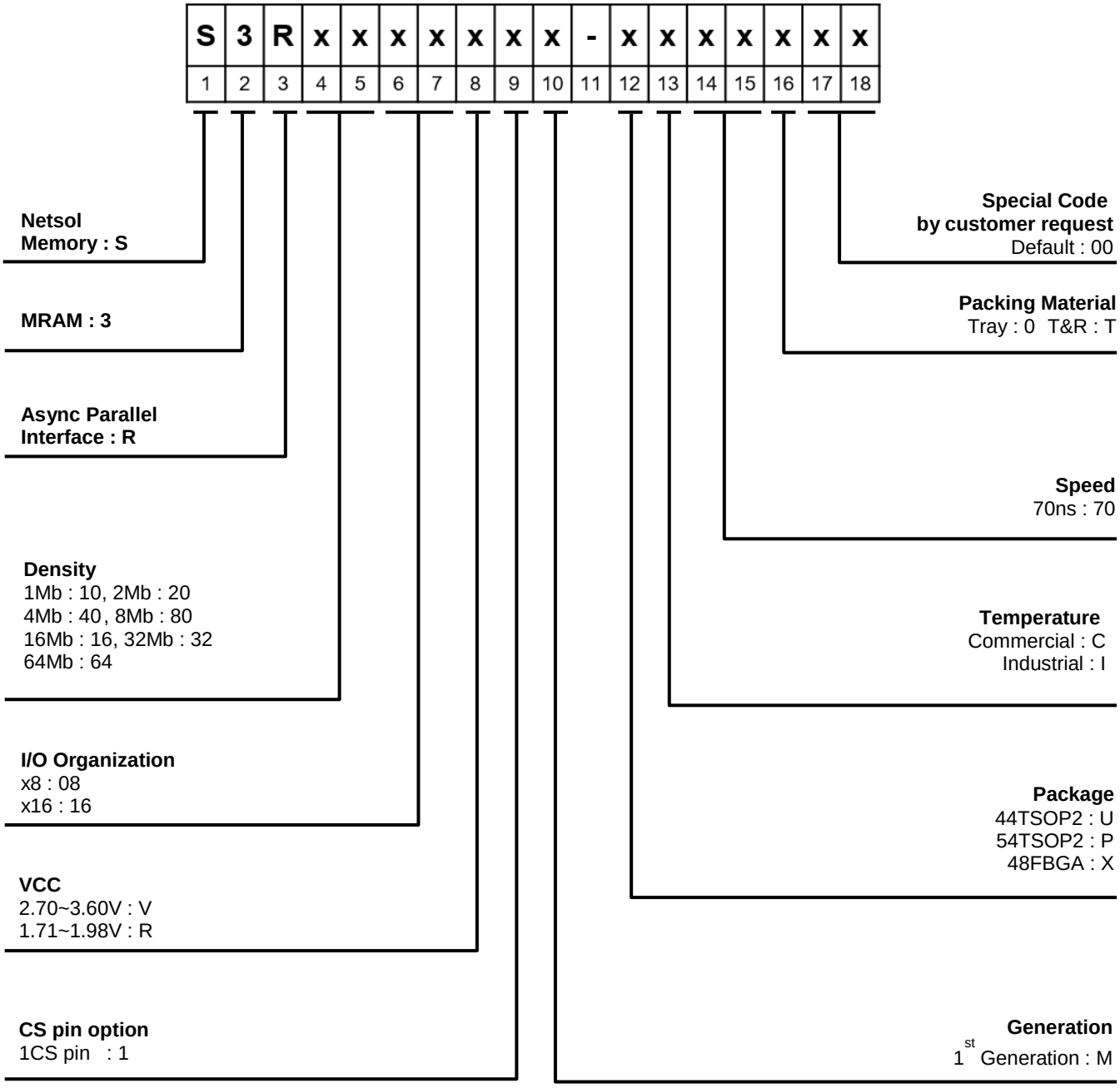
Thermal Resistance

Table 16 : Thermal Resistance

Parameter	Description	48FBGA	54TSOP2	Unit
θ_{JA}	Thermal resistance (junction to ambient)	69.4	50.3	°C/W
θ_{JC}	Thermal resistance (junction to case)	31.1	14.4	

Notes:
1: These parameters are guaranteed by characterization; not tested in production

Part Numbering System



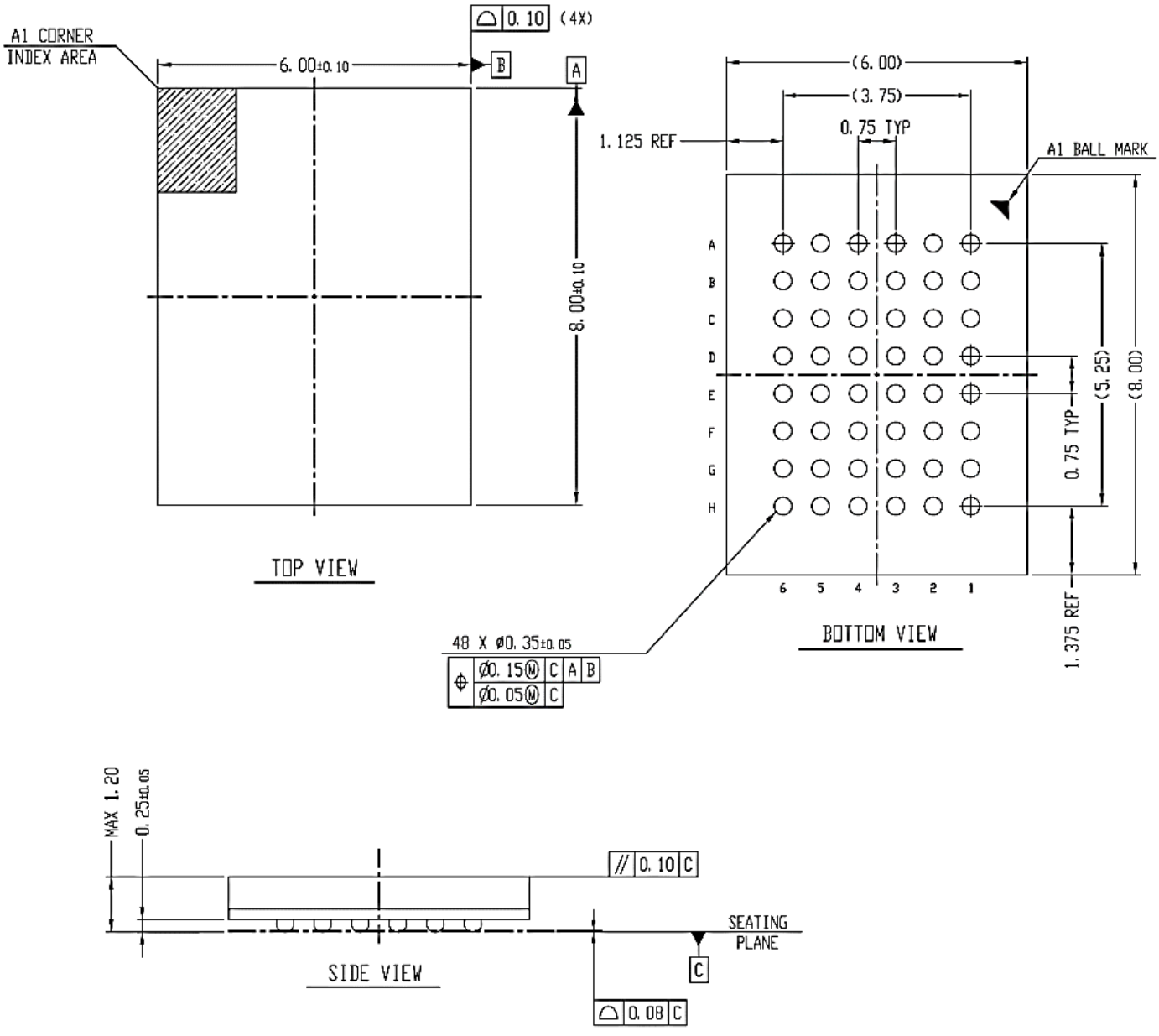
Ordering Part Numbers

Table 18 : Ordering Part Numbers

Density	Voltage	Temperature	Package	Packing Material	Part Number
32Mb	3.3V	-40°C ~ 85°C	54TSOP2	Tray	S3R3216V1M-PI70
				Tape and Reel	S3R3216V1M-PI70T
			48FBGA	Tray	S3R3216V1M-XI70
				Tape and Reel	S3R3216V1M-XI70T
	1.8V	-40°C ~ 85°C	54TSOP2	Tray	S3R3216R1M-PI70
				Tape and Reel	S3R3216R1M-PI70T
			48FBGA	Tray	S3R3216R1M-XI70
				Tape and Reel	S3R3216R1M-XI70T

Package Dimension

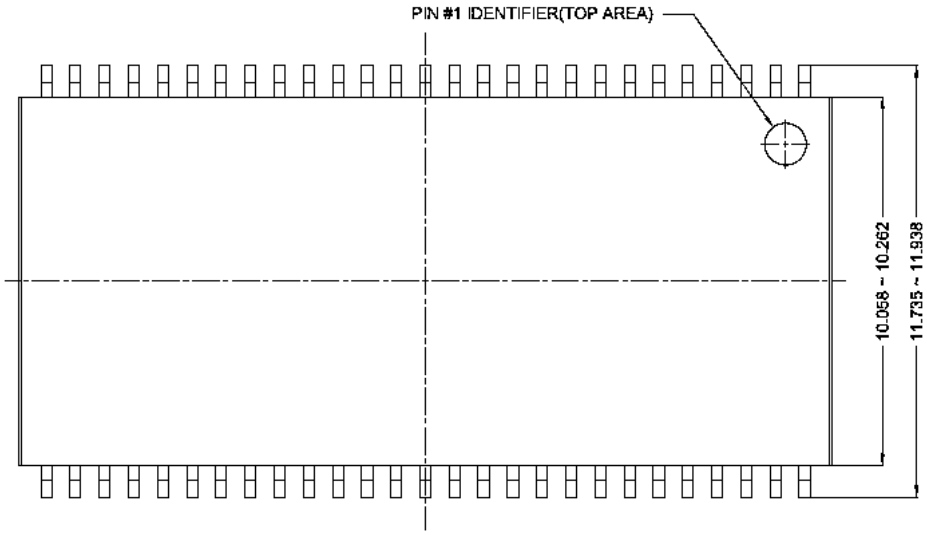
48 FBGA



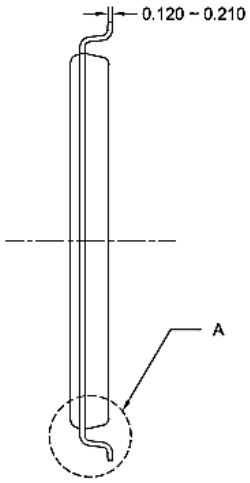
[Notes]

1. All Dimensions in Millimeters
2. Solder ball Diameter is post reflow diameter
   (Raw Solder ball size is Φ0.30mm)

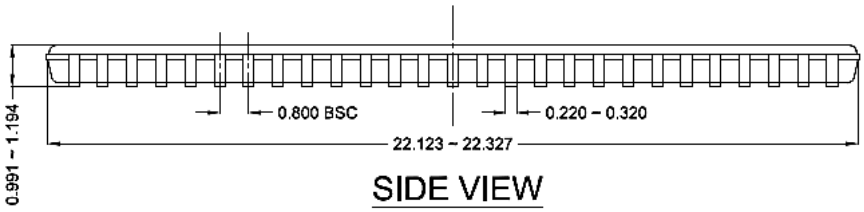
54 TSOP2



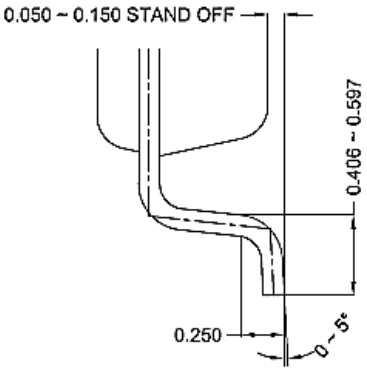
TOP VIEW



SIDE VIEW



SIDE VIEW



DETAIL "A"

[Notes]

1. Dimensions in Millimeters
2. Lead Finish : Solder Plated
3. Package dimensions refer to JEDEC MS-024

Revision History

Revision	Data	Description
0.0	Feb, 2023	Initial Release, Preliminary
1.0	Jul, 2023	1. Remove Preliminary status 2. Update DC characteristics(Table 10,11)