



2Mb Async. FAST SRAM B-die

Asynchronous FAST SRAM with ECC

1.65V ~ 3.6V

- **S6R2016WEB**
- **S6R2008WEB**

Datasheet

NETSOL RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.

Products and specifications discussed herein are for reference purposes only.
All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of NETSOL.
No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

For updates or additional information about Netsol products, please contact to netsol@netsol.co.kr

Features

- Fast Access Time : 8ns, 10ns, 12ns
- Embedded ECC
 - Single Bit Error Correction
- Wide range of Power Supply
 - 1.65V ~ 3.6V
- TTL Compatible Inputs and Outputs
- Three State Outputs
- Data Byte Control(x16 Mode)
 - $\overline{\text{LB}}$: I/O7~ I/O0, $\overline{\text{UB}}$: I/O15~ I/O8
- Standard 44 TSOP2 Package
- ROHS compliant
- Operating in Industrial Temperature range

Performance

Operation	Symbol	Typical Value			Unit
		3.3V	2.5V	1.8V	
Read Cycle Time	t_{RC}	8/10(min.)	10(min.)	12(min.)	ns
Address Access Time	t_{AA}	8/10(min.)	10(min.)	12(min.)	ns
Write Cycle Time	t_{WC}	8/10(min.)	10(min.)	12(min.)	ns
Standby Current	I_{SB1}	2.5	2.5	2.5	mA
Operating Current	I_{CC}	23/21	21	19	mA

Table of contents

Features	2
Performance	2
Table of contents.....	3
General Description	4
Asynchronous FAST SRAM Ordering Information	4
Logic Block Diagram – S6R2016WEB (128K x16)	5
Logic Block Diagram – S6R2008WEB (256K x8)	5
44TSOP2 Package Pin Configuration (Top View) – S6R2016WEB (128K x16)	6
44TSOP2 Package Pin Configuration (Top View) – S6R2008WEB (256K x8)	6
Absolute Maximum Ratings.....	7
Recommended DC Operating Conditions	7
DC and Operating Characteristics	8
Pin Capacitance.....	8
Test Conditions	9
Functional Description (x16 Mode)	10
Functional Description (x8 Mode)	10
Data Retention Characteristics.....	10
Data Retention Wave Form (CS Controlled)	10
AC Timing Parameters.....	11
Read Cycle	11
Write Cycle	11
Timing Diagrams	12
Timing Waveform of Read Cycle(1)	12
Timing Waveform of Read Cycle(2)	12
Timing Waveform of Write Cycle(1).....	13
Timing Waveform of Write Cycle(2).....	13
Timing Waveform of Write Cycle(3).....	14
Timing Waveform of Write Cycle(4).....	14
Package Dimensions.....	15
44-TSOP2-400BF.....	15
Revision History	16

General Description

The S6R2016WEB and S6R2008EB are a 2,097,152-bit high-speed Static Random Access Memory organized as 128K (256K) words by 16(8) bits. The S6R2016WEB (S6R2008WEB) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle. And S6R2016WEB allows that lower and upper byte access by data byte control($\overline{LB}$, $\overline{UB}$). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology.

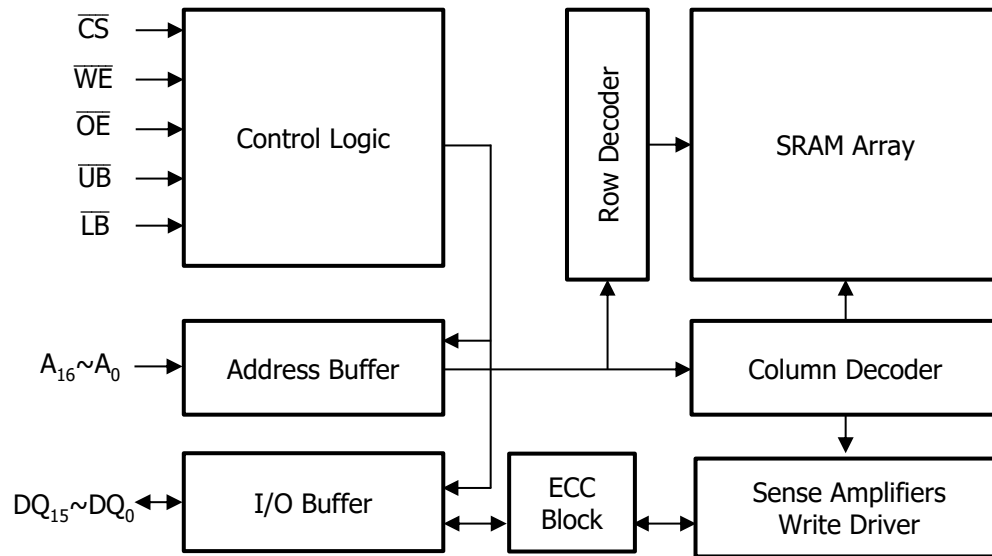
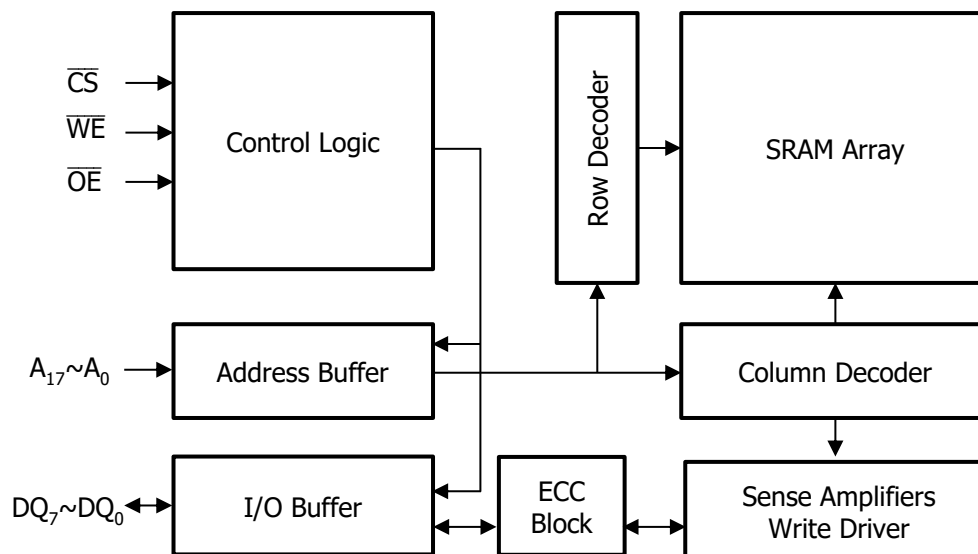
Single error correction logic is implemented for high reliability in devices. ECC logic can correct single bit error in read operation.

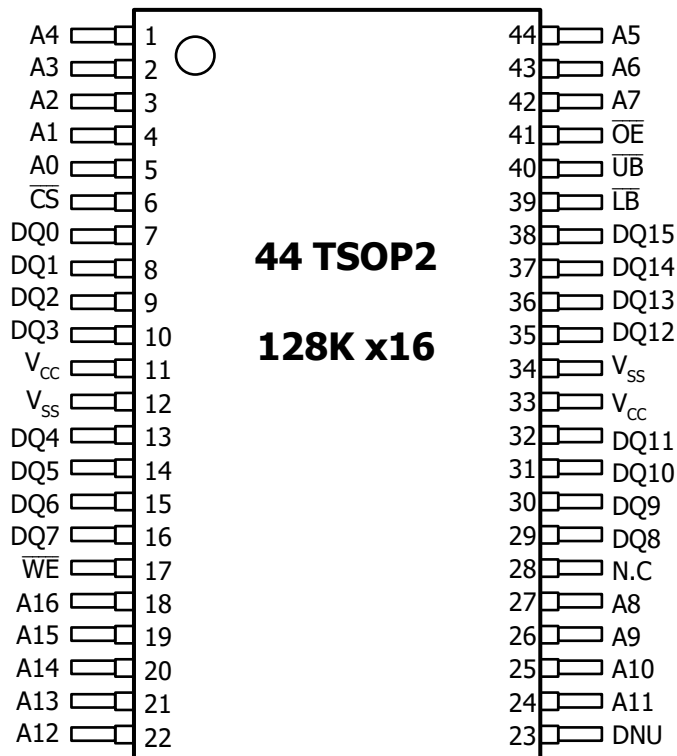
It is particularly well suited for use in high-reliable and high-speed system applications.

The S6R2016WEB and S6R2008WEB are packaged in a 400mil 44-pin TSOP2.

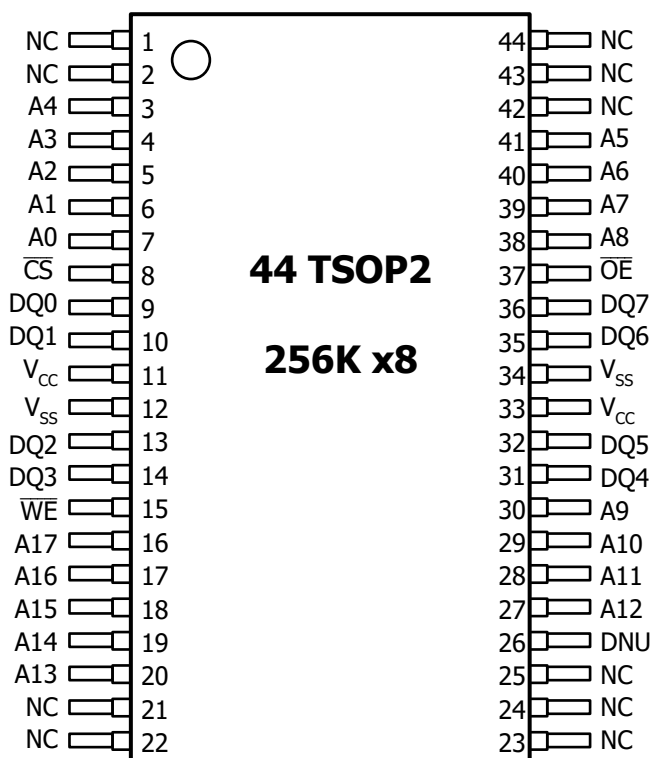
Asynchronous FAST SRAM Ordering Information

Density	Org.	Part Number	Vcc(V)	Speed (ns)		Package	Temperature
				tAA	tOE		
2Mb	128K x16	S6R2016WEB-UI08	3.3	8	4	44TSOP2	Industrial Temperature
			2.5	10	5		
			1.8	12	6		
		S6R2016WEB-UI10	3.3	10	5	44TSOP2	
			2.5	10	5		
			1.8	12	6		
	256K x8	S6R2008WEB-UI08	3.3	8	4	44TSOP2	
			2.5	10	5		
			1.8	12	6		
		S6R2008WEB-UI10	3.3	10	5	44TSOP2	
			2.5	10	5		
			1.8	12	6		

Logic Block Diagram – S6R2016WEB (128K x16)

Logic Block Diagram – S6R2008WEB (256K x8)


44TSOP2 Package Pin Configuration (Top View) – S6R2016WEB (128K x16)

Pin Function

Pin Name	Pin Function
A ₁₆ ~A ₀	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(DQ ₇ ~ DQ ₀)
$\overline{UB}$	Upper-byte Control(DQ ₁₅ ~ DQ ₈)
DQ ₁₅ ~DQ ₀	Data Inputs/Outputs
VCC	Power
VSS	Ground
NC	No Connection
DNU	Do Not Use : DNUs must be left unconnected.

44TSOP2 Package Pin Configuration (Top View) – S6R2008WEB (256K x8)

Pin Function

Pin Name	Pin Function
A ₁₇ ~A ₀	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
DQ ₇ ~DQ ₀	Data Inputs/Outputs
VCC	Power
VSS	Ground
NC	No Connection
DNU	Do Not Use : DNUs must be left unconnected.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Voltage on Vcc Supply Relative to VSS	V _{in} , V _{out}	-0.5 to V _{cc} +0.5V	V
Voltage on Any Pin Relative to VSS	V _{in} , V _{out}	-0.5 to 4.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	P _{STG}	-65 to 150	°C
Operating Ambient Temperature	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Operating Vcc(V)	Symbol	Min.	Typ.	Max.	Units
Vcc Supply Voltage	2.3 ~ 3.6	V _{cc}	2.3	2.5/3.3	3.6	V
	1.65 ~ 2.2	V _{cc}	1.65	1.8	2.2	V
Ground		V _{ss}	0	0	0	V
Input High Voltage	2.3 ~ 3.6	V _{IH}	2.0	-	V _{cc} +0.3	V
	1.65 ~ 2.2	V _{IH}	1.4	-	V _{cc} +0.2	V
Input Low Voltage	2.3 ~ 3.6	V _{IL}	-0.3	-	0.7	V
	1.65 ~ 2.2	V _{IL}	-0.2	-	0.4	V

DC and Operating Characteristics

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS} \text{ to } V_{CC}$	-2	-	+2	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT} = V_{SS} \text{ to } V_{CC}$	-2	-	+2	μA
Operating Current	I_{CC}	$V_{CC}(\text{max}), f=f_{\text{max}}, I_{OUT}=0\text{mA}$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	8ns	-	23	32
			10ns	-	21	30
			12ns	-	19	28
Standby Current	I_{SB}	$V_{CC}(\text{max}), f=f_{\text{max}}, \overline{CS} \geq V_{IH}$	-	-	15	mA
	I_{SB1}	$V_{CC}(\text{max}), f=0, \overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	2.5	9	
Output Low Voltage	V_{OL}	$V_{CC}=3.0V, I_{OL}=8\text{mA}$	-	-	0.4	V
		$V_{CC}=2.4V, I_{OL}=1\text{mA}$	-		0.4	
		$V_{CC}=1.65V, I_{OL}=0.1\text{mA}$	-		0.2	
Output High Voltage	V_{OH}	$V_{CC}=3.0V, I_{OH}=-4\text{mA}$	2.4	-	-	V
		$V_{CC}=2.4V, I_{OH}=-1\text{mA}$	1.8		-	
		$V_{CC}=1.65V, I_{OH}=-0.1\text{mA}$	1.4		-	

Pin Capacitance

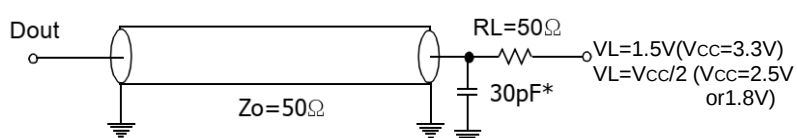
Item	Symbol	Test Conditions	Typ	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	-	8	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	-	6	pF

* $T_A=25^\circ C$, $f=1.0\text{MHz}$, Capacitance is sampled and not 100% tested.

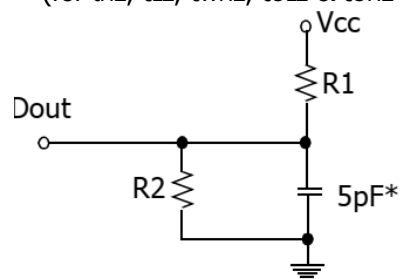
Test Conditions

Parameter	Value
Input Pulse Level	0 to 3.0V ($V_{CC}=3.3V$)
	0 to 2.5V ($V_{CC}=2.5V$)
	0 to 1.8V ($V_{CC}=1.8V$)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V ($V_{CC}=3.3V$)
	$1/2V_{CC}$ ($V_{CC}=2.5V$ or $1.8V$)
Output Load	See Fig. 1

Output Load (A)



Output Load(B)
(for tHZ, tLZ, tWHZ, tOLZ & tOHZ)



Vcc	3.3V	2.5V	1.8V
R1	319Ω	1909Ω	13500Ω
R2	353Ω	1105Ω	10800Ω

* Including Scope and Jig Capacitance

Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Modes	DQ Pins		Supply Current
						$DQ_7 \sim DQ_0$	$DQ_{15} \sim DQ_8$	
H	X	X*	X	X	Not Selected	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H		High-Z	High-Z	
L	H	L	L	H	Read	Dout	High-Z	I_{CC}
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	I_{CC}
			H	L		High-Z	Din	
			L	L		Din	Din	

* X means Don't Care.

Functional Description (x8 Mode)

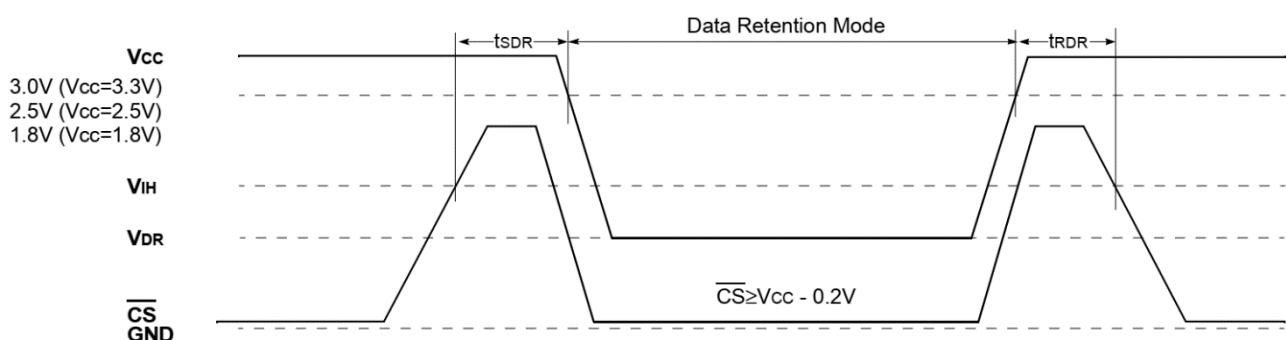
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Modes	DQ Pins	Supply Current
H	X*	X	Not Selected	High-Z	I_{SB}, I_{SB1}
L	H	H	Output disable	High-Z	I_{CC}
L	H	L	Word Read	Dout	I_{CC}
L	L	X	Word Write	Din	I_{CC}

* X means Don't Care.

Data Retention Characteristics

Parameter	Operating $V_{CC}(V)$	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	2.5/3.3	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
	1.8			1.5	-	-	
Data Retention Current	2.5/3.3	I_{DR}	$V_{CC}=2.0V$ $\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	2.5	9	mA
	1.8		$V_{CC}=1.5V$ $\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	2.5	9	
Data Retention Set-Up Time		tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time		tRDR		1	-	-	ms

Data Retention Wave Form ($\overline{CS}$ Controlled)



AC Timing Parameters

Read Cycle

Parameter	Symbol	8ns		10ns		12ns		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Enable to Output	t_{CO}	-	8	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	ns
$\overline{UB}$, $\overline{LB}$ Access Time ¹⁾	t_{BA}	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output ¹⁾	t_{BLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output ¹⁾	t_{BHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	8	-	10	-	12	ns

Notes:

- Those parameters are applied for x16 mode only.

Write Cycle

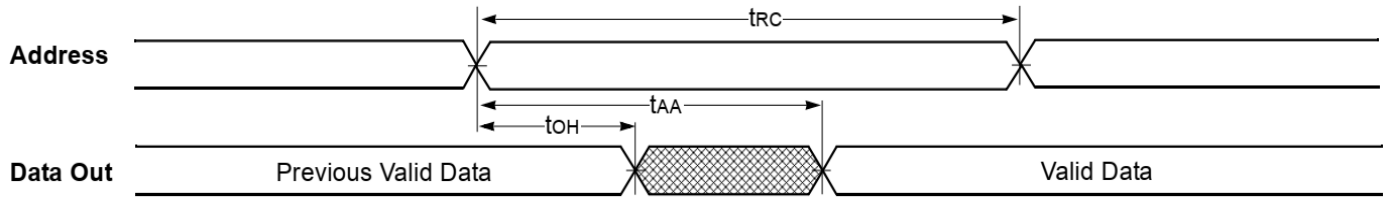
Parameter	Symbol	8ns		10ns		12ns		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	6	-	7	-	9	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP1}	8	-	10	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write ¹⁾	t_{BW}	6	-	7	-	9	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

Notes:

- Those parameters are applied for x16 mode only.

Timing Diagrams

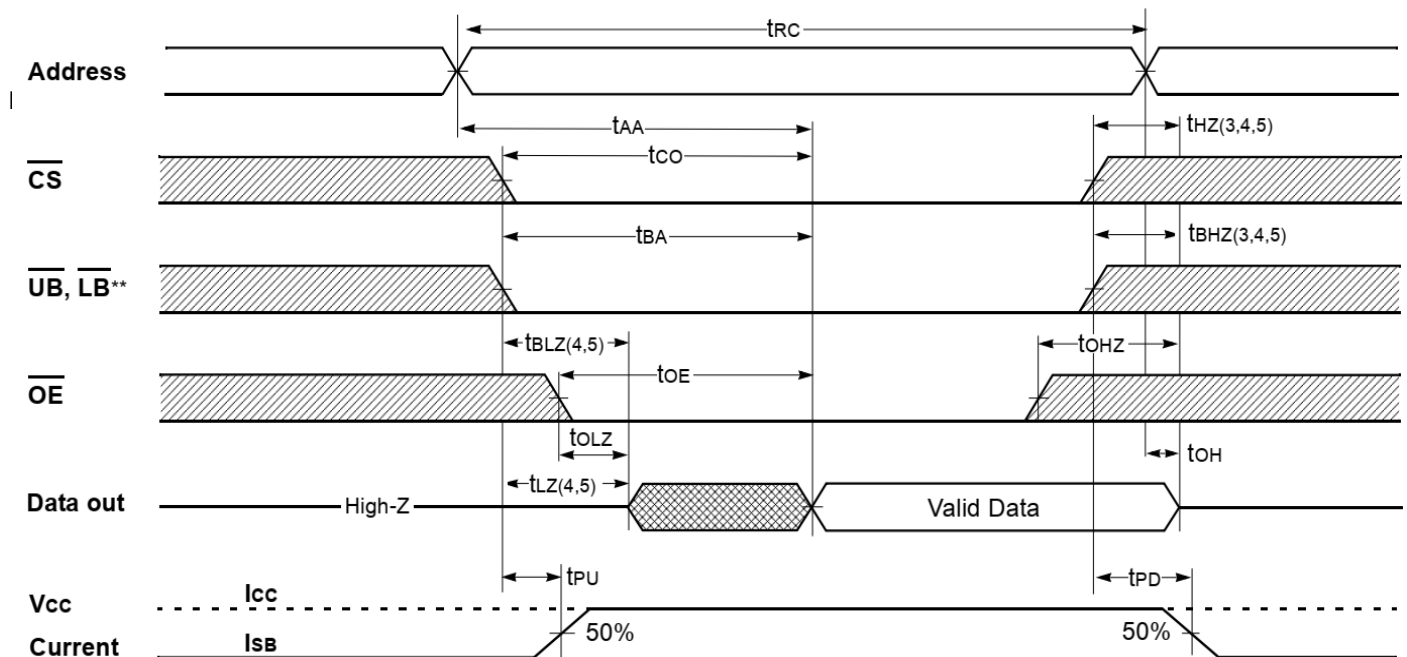
Timing Waveform of Read Cycle(1) (Address Controlled, $\overline{CS} = \overline{OE} = VIL$, $\overline{WE} = VIH$, $\overline{UB}$, $\overline{LB} = VIL$ ¹⁾)



Notes:

1. Those parameters are applied for x16 mode only.

Timing Waveform of Read Cycle(2) ($\overline{WE} = VIH$)

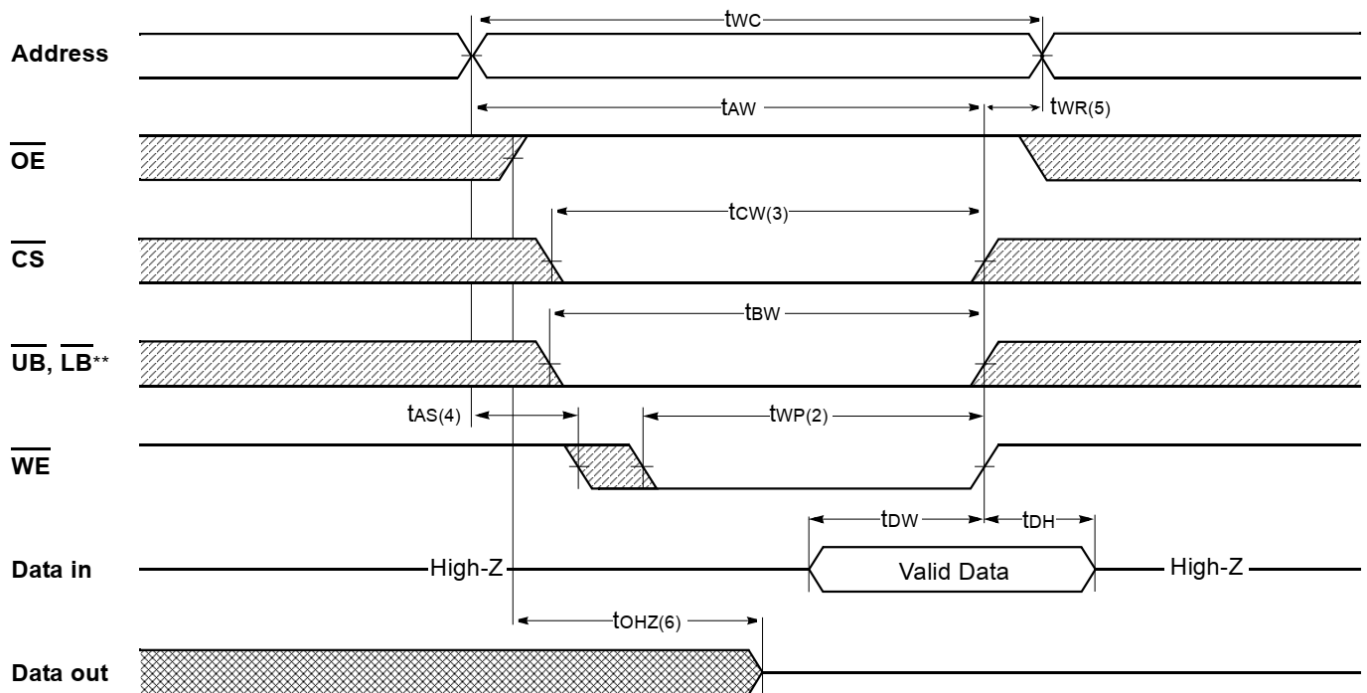


Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = VIL$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common DQ applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

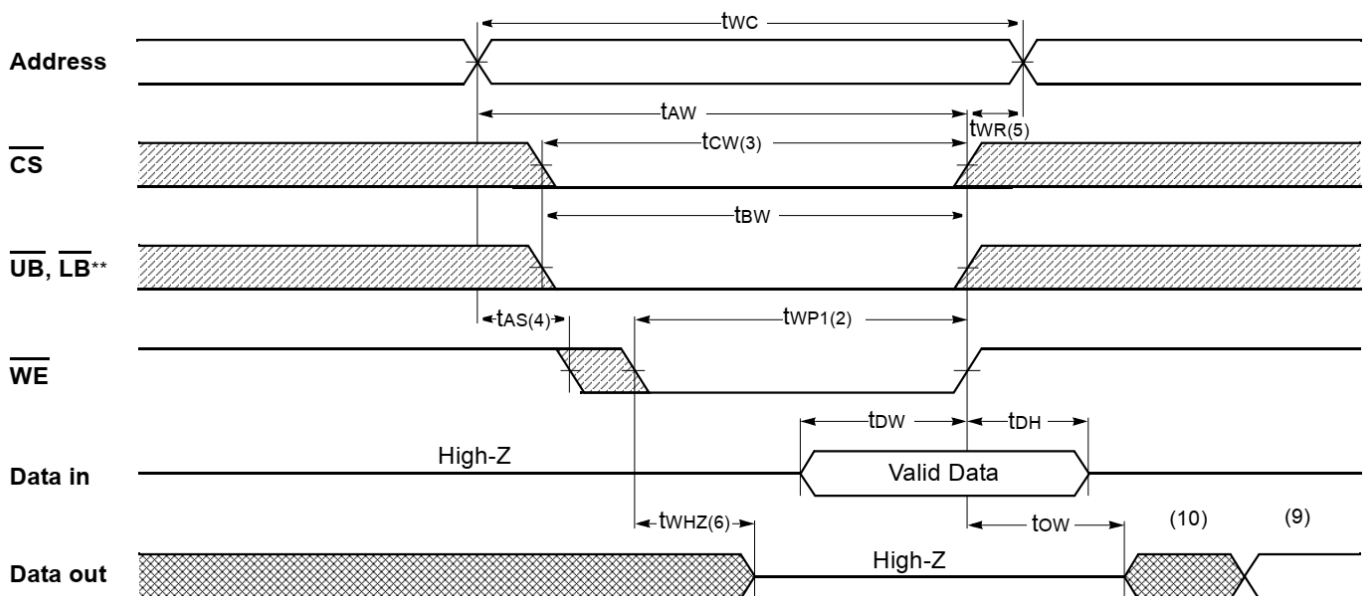
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(1) ($\overline{OE}$ Clock)



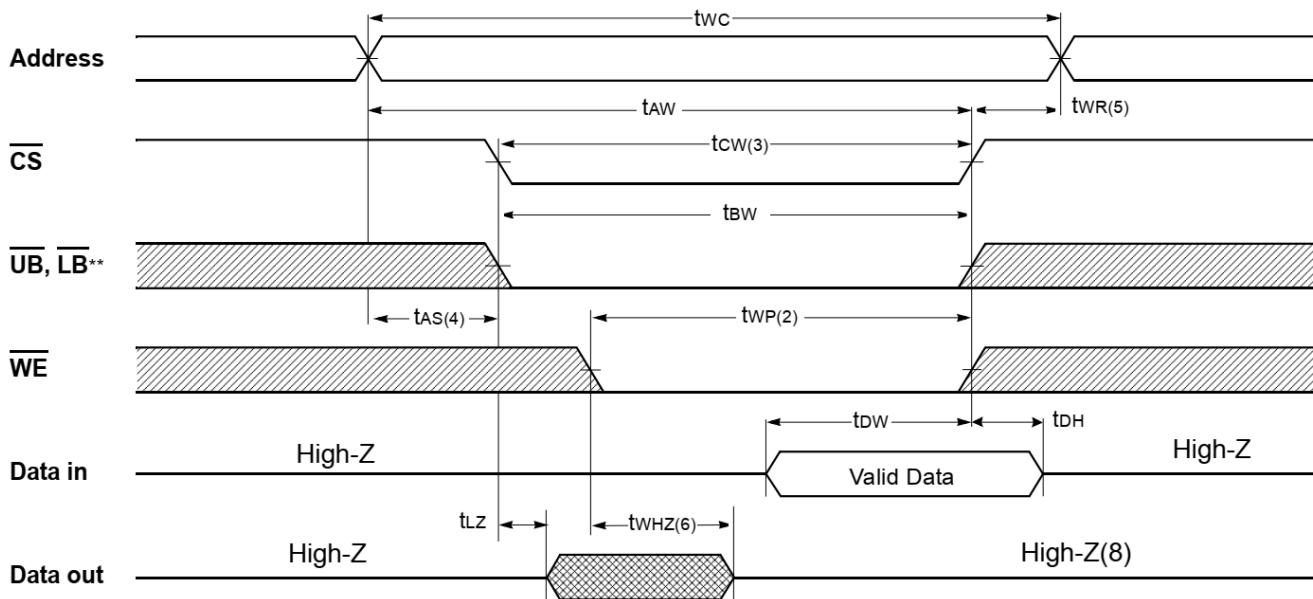
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(2) ($\overline{OE}$ = Low Fix)



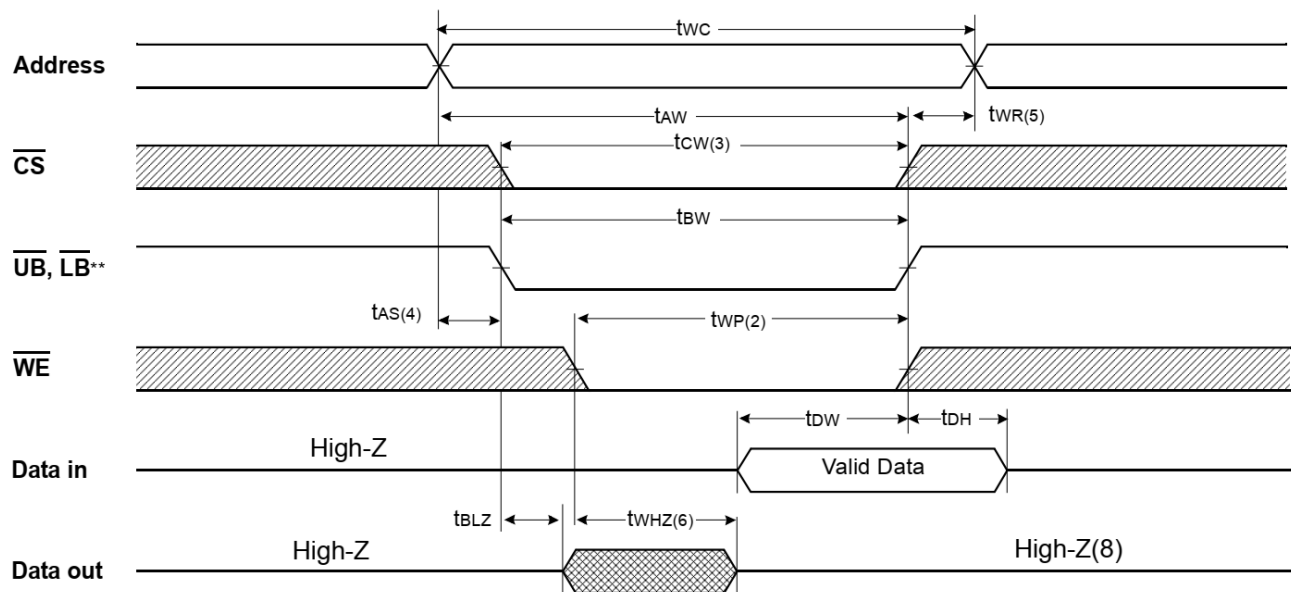
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(3) ($\overline{CS}$ Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



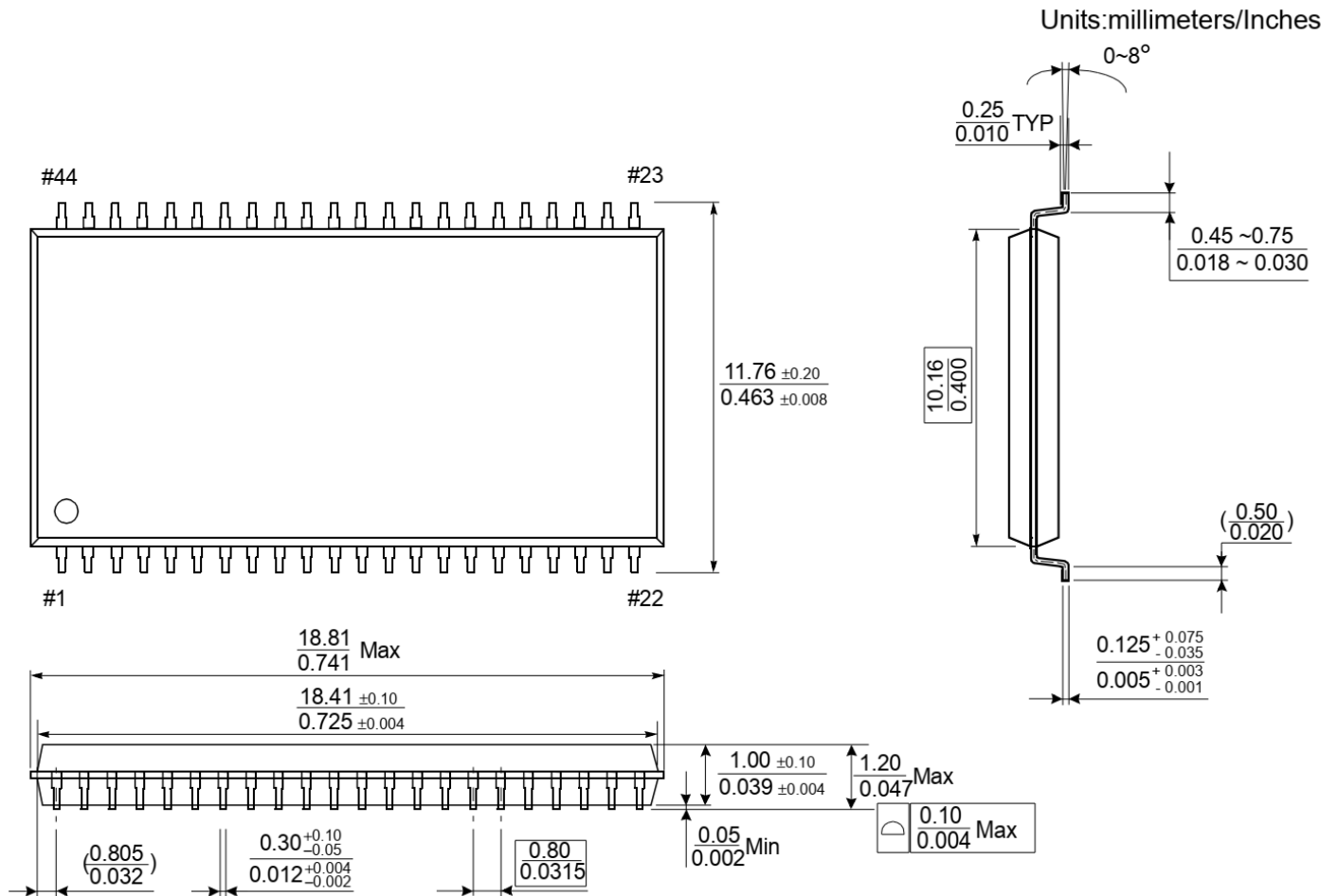
Notes (Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tcw is measured from the later of $\overline{CS}$ going low to end of write.
4. tas is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only.

Package Dimensions

44-TSOP2-400BF



Revision History

Revision	Date	Description
0.0	Jul. 2023	Initial Release, Preliminary
1.0	Nov. 2023	1. Remove Preliminary status 2. Update DC Characteristics