Application Note

1Mb ~ 32Mb SPI MRAM

- S3A1004V0M
- S3A2004V0M
- S3A4004V0M
- S3A8004V0M
- S3A1604V0M
- S3A3204V0M
- S3A1004R0M
- S3A2004R0M
- S3A4004R0M
- S3A8004R0M
- S3A1604R0M
- S3A3204R0M

Single/Dual/Quad IO SPI MRAM
3.3V/1.8V

Revision 1.0

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General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM). It features a SPI bus interface, XIP(execute-in-place) functionality, and hardware/software based data protection mechanisms. SPI (Serial Peripheral Interface) is a synchronous serial communication interface with command, address and data signals.

It requires less pin counts than parallel interface and is easy to be configured on the system. The device is offered in density ranging from 1Mbit to 32Mbit. The device can replace Flash, FRAM or (nv)SRAM with same functionality and non-volatility.

Table 1 : Part Number

Density	3.3V Product	1.8V Product
32Mb	S3A3204V0M	S3A3204R0M
16Mb	S3A1604V0M	S3A1604R0M
8Mb	S3A8004V0M	S3A8004R0M
4Mb	S3A4004V0M	S3A4004R0M
2Mb	S3A2004V0M	S3A2004R0M
1Mb	S3A1004V0M	S3A1004R0M

Solder Reflow

Netsol recommends the solder reflow condition as follows :
1. The peak temperature must not exceed 260 ℃.
2. The time above 255 ℃ must not exceed 30 seconds.
3. The reflow cycles must not exceed 3 times.

Table 2 : Solder Reflow Condition

Solder Reflow Process	Max.	Units
Reflow profiles	JEDEC J-STD-020 reflow profiles	
Peak Temperature	260°C	°C
Time above 255°C	30	seconds
Reflow cycles	3	times

Initialization for Nonvolatile Register

The device has nonvolatile register bits – status register, configuration register, serial number register, augmented 256-byte area and protection register for augmented 256-byte area. ***These register bits are required to be set at least once on power-up after high temperature solder reflow process.***

Netsol recommends the following sequence.

1. power-on
   - SSPI mode is enabled after power-on, software reset or JEDEC reset.
   - Please refer to the power-on sequence in the datasheet.
2. Write the configuration registers
   - $\overline{WP}$ =H, WREN(06h) + WRCX[87h + 4 bytes data: CR1(00h), CR2(0xh), CR3(xxh), CR4(xxh)]
   - Users can set CR1, CR2, CR3 and CR4 to the values to be used.
   - CR1(00h) makes SR[5:2] and augmented 256-byte area protection register writable.
3. Write the status register
   - $\overline{WP}$ =H, WREN(06h) + WRSR[01h + 1 byte data: SR(00h)]
4. Write the augmented 256-byte area protection register
   - $\overline{WP}$ =H, WREN(06h) + WRAP[1Ah + 1 byte data: 00h]
5. Users can check the register values using read register instructions.

Table 3 : Status Register-Data Protection

Bits	Name	Read/ Write	Initialization State	Description
SR[7]	WPEN	R/W	0	Hardware Based $\overline{WP}$ Protect Bit 1: Protection Enabled – write protects when $\overline{WP}$ is Low 0: Protection Disabled – Doesn't write protect when $\overline{WP}$ is Low
SR[6]	SNPEN	R/W	0	Serial Number Protect Bit 1: Serial Number Write protected 0: Serial Number Writable
SR[5]	TB	R/W	0	Top/Bottom Memory Array Protect Selection 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BP[2]	R/W	0	Block Protection Bits
SR[3]	BP[1]	R/W	0	
SR[2]	BP[0]	R/W	0	
SR[1]	WREN	R	0	Write Protection Enable 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	R	-	Reserved for future use

Note : SR[7:2] are nonvolatile bits.

Table 4 : Augmented 256-Byte Area Protection Register : 1Mb ~ 16Mb

Bits	Name	Address Range	Read/ Write	Initialization State	Description
ASP[7]	ASPS[7]	0000E0h – 0000FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	0000C0h – 0000DFh		0	
ASP[5]	ASPS[5]	0000A0h – 0000BFh		0	
ASP[4]	ASPS[4]	000080h – 00009Fh		0	
ASP[3]	ASPS[3]	000060h – 00007Fh		0	
ASP[2]	ASPS[2]	000040h – 00005Fh		0	
ASP[1]	ASPS[1]	000020h – 00003Fh		0	
ASP[0]	ASPS[0]	000000h – 00001Fh		0	

Table 5 : Augmented 512-Byte Area Protection Register : 32Mb

Bits	Name	Address Range	Read/ Write	Default State	Description
ASP[7]	ASPS[7]	0001C0h – 0001FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	000180h – 0001BFh	R/W	0	
ASP[5]	ASPS[5]	000140h – 00017Fh	R/W	0	
ASP[4]	ASPS[4]	000100h – 00013Fh	R/W	0	
ASP[3]	ASPS[3]	0000C0h – 0000FFh	R/W	0	
ASP[2]	ASPS[2]	000080h – 0000BFh	R/W	0	
ASP[1]	ASPS[1]	000040h – 00007Fh	R/W	0	
ASP[0]	ASPS[0]	000000h – 00003Fh	R/W	0	

Note : ASP[7:0] are nonvolatile bits.

Table 6 : Configuration Register 1

Bits	Name	Read/ Write	Initialization State	Selection Options
CR1[7]	RSVD	R/W	0	Reserved for future use
CR1[6]	RSVD		0	Reserved for future use
CR1[5]	RSVD		0	Reserved for future use
CR1[4]	RSVD		0	Reserved for future use
CR1[3]	RSVD		0	Reserved for future use
CR1[2]	MAPLK		0	Status Register TB, BP[2:0] Protect 1: Lock TB and BP[2:0] 0: Unlock TB and BP[2:0]
CR1[1]	RSVD		0	Reserved for future use
CR1[0]	ASPLK		0	Augmented 256-Byte Area Data Protection 1: Write Protection for Augmented Area Data regardless of ASP[7:0] 0: Write Protection for Augmented Area Data depending on ASP[7:0]

Note : CR1[7:0] are nonvolatile bits.

Table 7 : Configuration Register 2

Bits	Name	Read/ Write	Initialization State	Description
CR2[7]	RSVD	R/W	0	Reserved for future use
CR2[6]	QPIEN	R	0	Quad SPI (QPI 4-4-4) Interface Mode 1: Quad SPI (QPI 4-4-4) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[5]	RSVD	R/W	0	It must be written as 0
CR2[4]	DPIEN	R	0	Dual SPI (DPI 2-2-2) Interface Mode 1: Dual SPI (DPI 2-2-2) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[3]	RL[3]	R/W	User selection	Read Latency Selection Bits : CR2[3:0] 0000: 0 Cycle 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	RL[2]	R/W	User selection	
CR2[1]	RL[1]	R/W	User selection	
CR2[0]	RL[0]	R/W	User selection	

Notes :
1. Read Latency is frequency dependent.
2. Read(03h) does not depend on Read latency Selection Bits, CR2[3:0].
3. CR2[7,5,3:0] are nonvolatile bits.

Table 8 : Configuration Register 3

Bits	Name	Read/ Write	Initialization State	Description
CR3[7]	DRV[2]	R/W	User selection	Output Driver Strength Selection DRV[2:0] 3.3V 1.8V 000: 36Ω 35Ω 001: 100Ω 95Ω 010: 75Ω 63Ω 011: 60Ω 50Ω 100: 48Ω 40Ω 101: 41Ω 30Ω 110: 29Ω 26Ω 111: 24Ω 22Ω
CR3[6]	DRV[1]		User selection	
CR3[5]	DRV[0]		User selection	
CR3[4]	WRPEN		User selection	Read WRAP Enable 1: Read Wrap Enabled 0: Read Wrap Disabled
CR3[3]	RSVD		0	Reserved for future use
CR3[2]	WRPL[2]		User selection	Wrap length configuration WRPL[2:0] 000: 16-byte wrap 001: 32-byte wrap 010: 64-byte wrap 011: 128-byte wrap 100: 256-byte wrap 101: 512-byte wrap 110: 1K-byte wrap 111: Reserved
CR3[1]	WRPL[1]		User selection	
CR3[0]	WRPL[0]		User selection	

Notes :
1. Default output strength is DRV[2:0]=000.
2. CR4[7:0] are nonvolatile bits.

Table 9 : Configuration Register 4

Bits	Name	Read/ Write	Initialization State	Selection Options
CR4[7]	RSVD	R/W	0	Reserved for future use
CR4[6]	RSVD		0	Reserved for future use
CR4[5]	RSVD		0	Reserved for future use
CR4[4]	RSVD		0	Reserved for future use
CR4[3]	RSVD		0	Reserved for future use
CR4[2]	RSVD		0	Reserved for future use
CR4[1]	WRENS[1]		User selection	00: Normal: WREN is prerequisite to all Memory Array and Augmented 256-byte Area Write instruction. (WREN is reset after $\overline{CS}$ goes High) 01: SRAM: WREN is not a prerequisite to Memory Array and Augmented 256-byte Area Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write or Augmented 256-byte Area instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset after $\overline{CS}$ goes High) 11: Reserved
CR4[0]	WRENS[0]		User selection	

Notes :

1. Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write Instructions require WREN to be set and WREN resets once $\overline{CS}$ goes High for the write instruction.
   CR4[1:0] only affects the writing for memory and augmented 256-bytes area.
2. CR4[7:0] are nonvolatile bits.

Revision History

Revision	Data	Description
0.0	May, 2022	Initial Release, Preliminary
0.1	Jan, 2023	Add 32Mb density
1.0	Feb, 2023	Removed Preliminary status

* Products and specifications discussed herein are subject to change by Netsol without notice.