Preliminary

8Mb Async. FAST SRAM B-die

Asynchronous FAST SRAM with ECC

1.65V ~ 3.6V

- **S6R8016WEB**
- **S6R8008WEB**

Datasheet

Features

- Fast Access Time : 8ns, 10ns, 12ns
- Embedded ECC
  - Single Bit Error Correction
- Wide range of Power Supply
  - 1.65V ~ 3.6V
- TTL Compatible Inputs and Outputs
- Three State Outputs
- Data Byte Control(x16 Mode)
  $\overline{LB}$: I/O0~ I/O7, $\overline{UB}$: I/O8~ I/O15
- Standard 44 TSOP2 and 48FBGA Package
- ROHS compliant
- Operating in Industrial Temperature range

Performance

Operation	Symbol	Typical Value			Unit
		3.3V	2.5V	1.8V	
Read Cycle Time	t_{RC}	8/10(min.)	10(min.)	12(min.)	ns
Address Access Time	t_{AA}	8/10(min.)	10(min.)	12(min.)	ns
Write Cycle Time	t_{WC}	8/10(min.)	10(min.)	12(min.)	ns
Standby Current	I_{SB}	5.0	5.0	5.0	mA
Operating Current	I_{CC}	45/40	40	36	mA

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General Description

The S6R8016WEB and S6R8008WEB are a 8,388,608-bit high-speed Static Random Access Memory organized as 512K (1M) words by 16(8) bits. The S6R8016WEB (S6R8008WEB) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle. And S6R8016WEB allows that lower and upper byte access by data byte control($\overline{LB}$, $\overline{UB}$). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology.

Single error correction logic is implemented for high reliability in devices. ECC logic can correct single bit error in read operation.

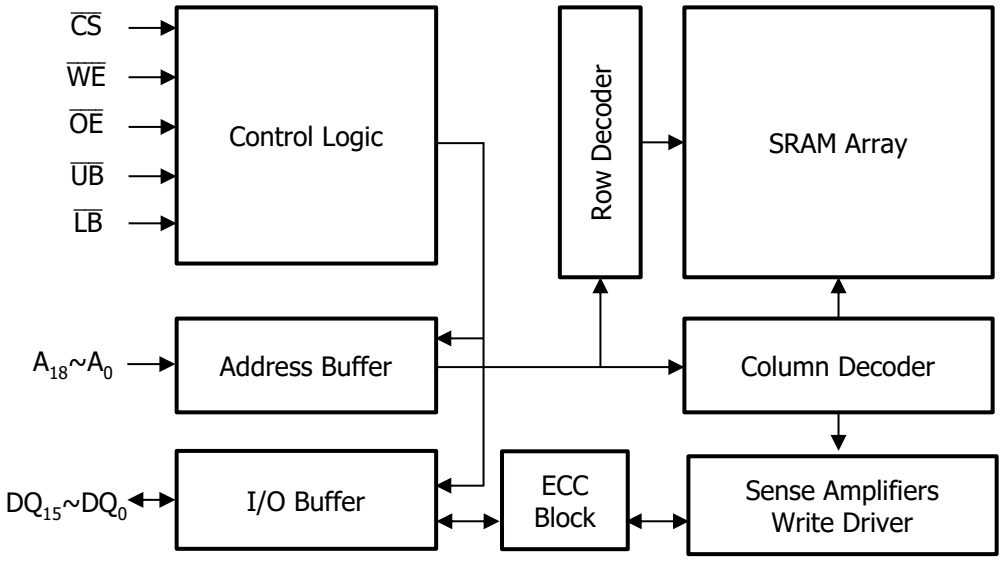
It is particularly well suited for use in high-reliable and high-speed system applications.

The S6R8016WEB and S6R8008WEB are packaged in a 400mil 44-pin TSOP2 and 48 Ball FBGA.

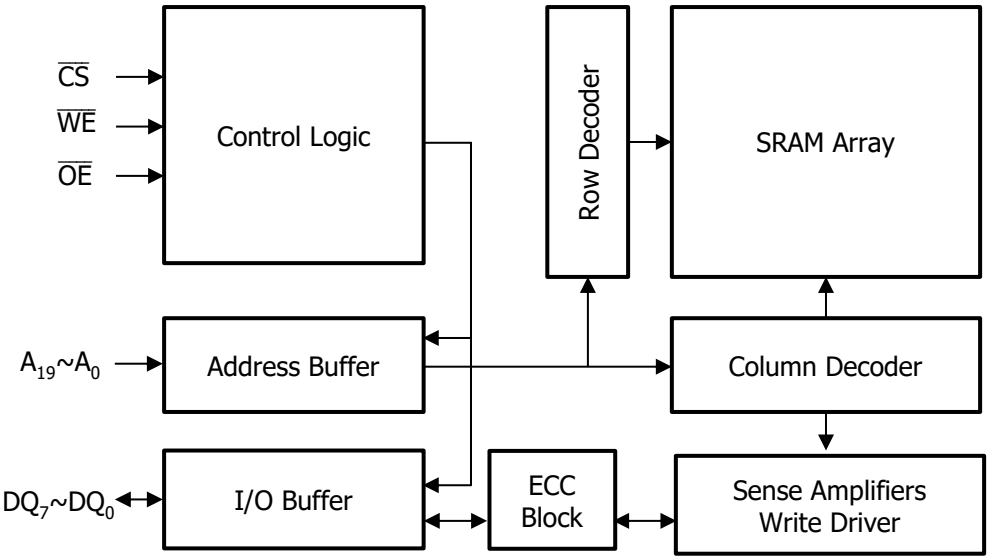
Asynchronous FAST SRAM Ordering Information

Density	Org.	Part Number	Vcc(V)	Speed (ns)		Package	Temperature
				tAA	tOE		
8Mb	512K x16	S6R8016WEB-XI08	3.3	8	4	48FBGA	Industrial Temperature
			2.5	10	5		
			1.8	12	6		
		S6R8016WEB-XI10	3.3	10	5	48FBGA	
			2.5	10	5		
			1.8	12	6		
	1M x8	S6R8008WEB-UI08	3.3	8	4	44TSOP2	
			2.5	10	5		
			1.8	12	6		
		S6R8008WEB-UI10	3.3	10	5	44TSOP2	
			2.5	10	5		
			1.8	12	6		

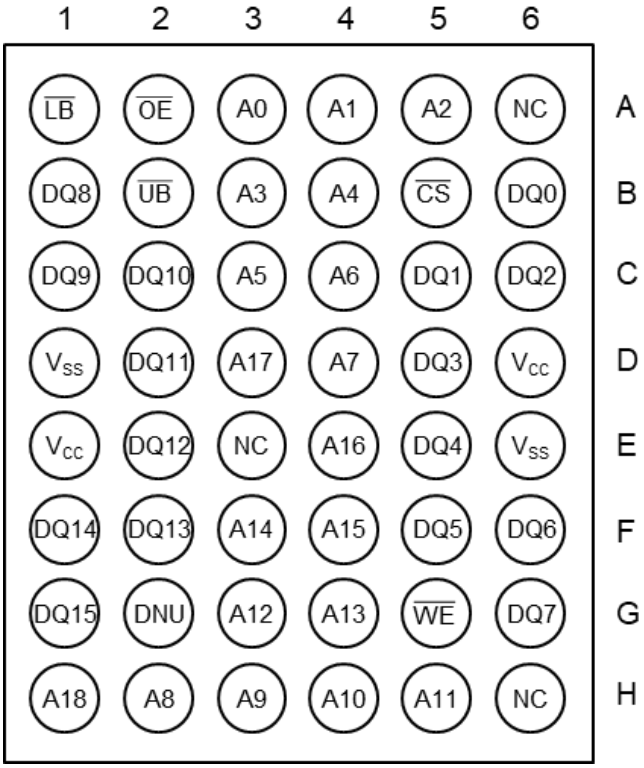
Logic Block Diagram – S6R8016WEB (512K x16)



Logic Block Diagram – S6R8008WEB (1M x8)



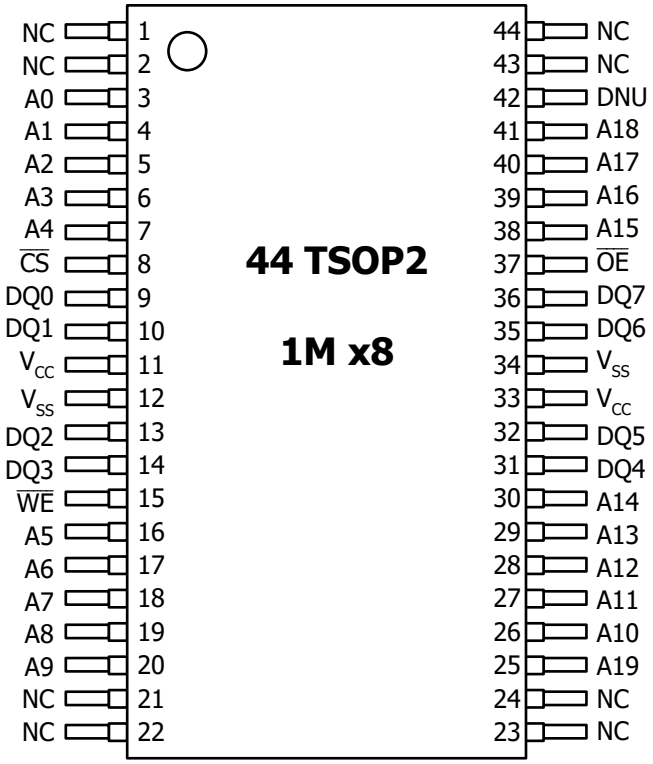
48FBGA Package Pin Configuration (Top View) – S6R8016WEB (512K x16)



Pin Function

Pin Name	Pin Function
A_{18}~A_0	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(DQ0~DQ7)
$\overline{UB}$	Upper-byte Control(DQ8~DQ15)
DQ_{15}~DQ_0	Data Inputs/Outputs
VCC	Power
VSS	Ground
NC	No Connection
DNU	Do Not Use : DNUs must be left unconnected.

44TSOP2 Package Pin Configuration (Top View) – S6R8008WEB (1M x8)



Pin Function

Pin Name	Pin Function
A_{19}~A_0	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
DQ_7~DQ_0	Data Inputs/Outputs
VCC	Power
VSS	Ground
NC	No Connection
DNU	Do Not Use : DNUs must be left unconnected.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Voltage on Vcc Supply Relative to VSS	Vin, Vout	-0.5 to Vcc+0.5V	V
Voltage on Any Pin Relative to VSS	Vin, Vout	-0.5 to 4.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	P_{STG}	-65 to 150	°C
Operating Ambient Temperature	T_A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Operating Vcc(V)	Symbol	Min.	Typ.	Max.	Units
Vcc Supply Voltage	2.3 ~ 3.6	Vcc	2.3	2.5/3.3	3.6	V
	1.65 ~ 2.2	Vcc	1.65	1.8	2.2	V
Ground		Vss	0	0	0	V
Input High Voltage	2.3 ~ 3.6	V_{IH}	2.0	-	Vcc+0.3	V
	1.65 ~ 2.2	V_{IH}	1.4	-	Vcc+0.2	V
Input Low Voltage	2.3 ~ 3.6	V_{IL}	-0.3	-	0.7	V
	1.65 ~ 2.2	V_{IL}	-0.2	-	0.4	V

DC and Operating Characteristics

Parameters	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		-2	-	+2	uA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = V_{SS} to V_{CC}		-2	-	+2	uA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	8ns	-	45	65	mA
			10ns	-	40	60	
			12ns	-	36	55	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$≥V_{IH}		-	-	30	mA
	I_{SB1}	V_{CC} (max), $\overline{CS}$≥V_{CC}-0.2V		-	5	20	
Output Low Voltage	V_{OL}	V_{CC}=3.0V, I_{OL}=8mA		-	-	0.4	V
		V_{CC}=2.4V, I_{OL}=1mA		-		0.4	
		V_{CC}=1.65V, I_{OL}=0.1mA		-		0.2	
Output High Voltage	V_{OH}	V_{CC}=3.0V, I_{OH}=-4mA		2.4	-	-	V
		V_{CC}=2.4V, I_{OH}=-1mA		1.8		-	
		V_{CC}=1.65V, I_{OH}=-0.1mA		1.4		-	

Pin Capacitance

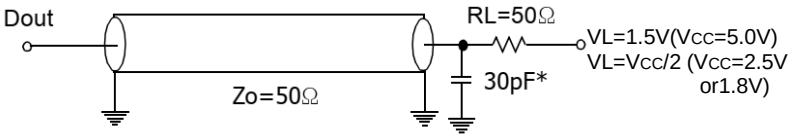
Item	Symbol	Test Conditions	Typ	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

* T_A=25°C, f=1.0MHz, Capacitance is sampled and not 100% tested.

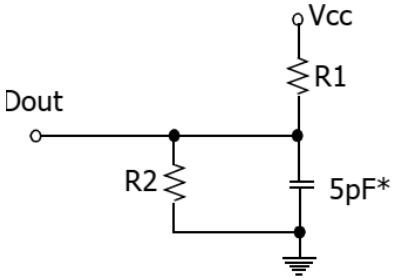
Test Conditions

Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V)
	0 to 2.5V (Vcc=2.5V)
	0 to 1.8V (Vcc=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V)
	1/2Vcc (Vcc=2.5V or 1.8V)
Output Load	See Fig. 1

Output Load (A)



Output Load(B)
(for tHZ, tLZ, tWHZ, tOLZ & tOHZ)



Vcc	3.3V	2.5V	1.8V
R1	319Ω	1909Ω	13500Ω
R2	353Ω	1105Ω	10800Ω

* Including Scope and Jig Capacitance

Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Modes	DQ Pins		Supply Current
						DQ_7~DQ_0	DQ_{15}~DQ_8	
H	X	X*	X	X	Not Selected	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-Z	I_{CC}
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	I_{CC}
			H	L		High-Z	Din	
			L	L		Din	Din	

* X means Don't Care.

Functional Description (x8 Mode)

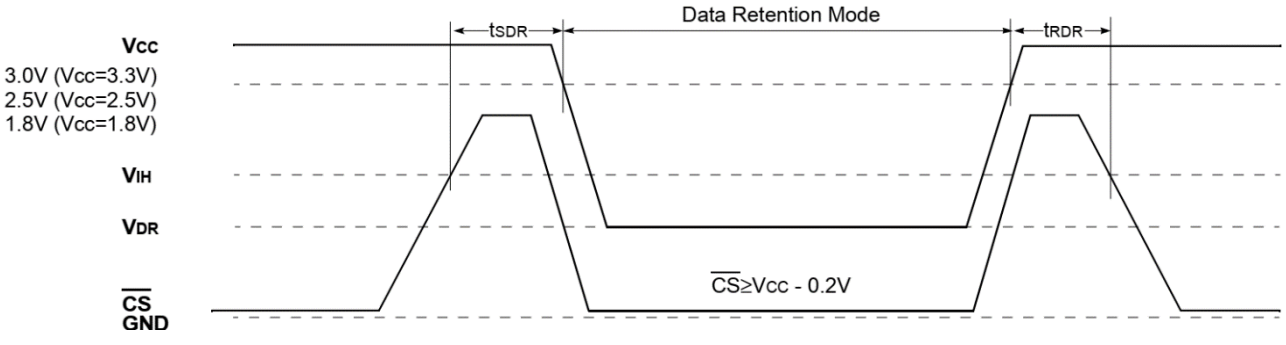
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Modes	DQ Pins	Supply Current
H	X*	X	Not Selected	High-Z	I_{SB}, I_{SB1}
L	H	H	Output disable	High-Z	I_{CC}
L	H	L	Word Read	Dout	I_{CC}
L	L	X	Word Write	Din	I_{CC}

* X means Don't Care.

Data Retention Characteristics

Parameter	Operating Vcc(V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Rention	2.5/3.3	V_{DR}	$\overline{CS}$≥Vcc – 0.2V	2.0	-	-	V
	1.8			1.5	-	-	
Data Retention Current	2.5/3.3	I_{DR}	Vcc=2.0V $\overline{CS}$≥Vcc–0.2V V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	-	5	20	mA
	1.8		Vcc=1.5V $\overline{CS}$≥Vcc–0.2V V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	-	5	20	
Data Retention Set-Up Time		tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time		tRDR		1	-	-	ms

Data Retention Wave Form ($\overline{CS}$ Controlled)



AC Timing Parameters

Read Cycle

Parameter	Symbol	8ns		10ns		12ns		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Enable to Output	t_{CO}	-	8	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	ns
$\overline{UB}$, $\overline{LB}$ Access Time [1)]	t_{BA}	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output [1)]	t_{BLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output [1)]	t_{BHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t_{PD}	-	8	-	10	-	12	ns

Notes:
1. Those parameters are applied for x16 mode only.

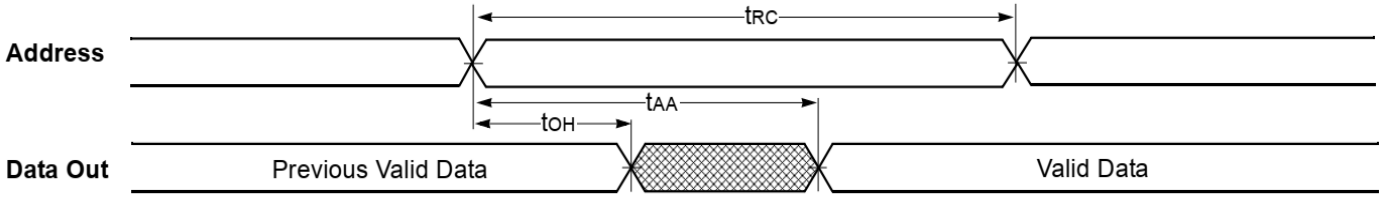
Write Cycle

Parameter	Symbol	8ns		10ns		12ns		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	6	-	7	-	9	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6	-	7	-	9	-	ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP1}	8	-	10	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write [1)]	t_{BW}	6	-	7	-	9	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Ouput High-Z	t_{WHZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End of Write to Ouput Low-Z	t_{OW}	3	-	3	-	3	-	ns

Notes:
1. Those parameters are applied for x16 mode only.

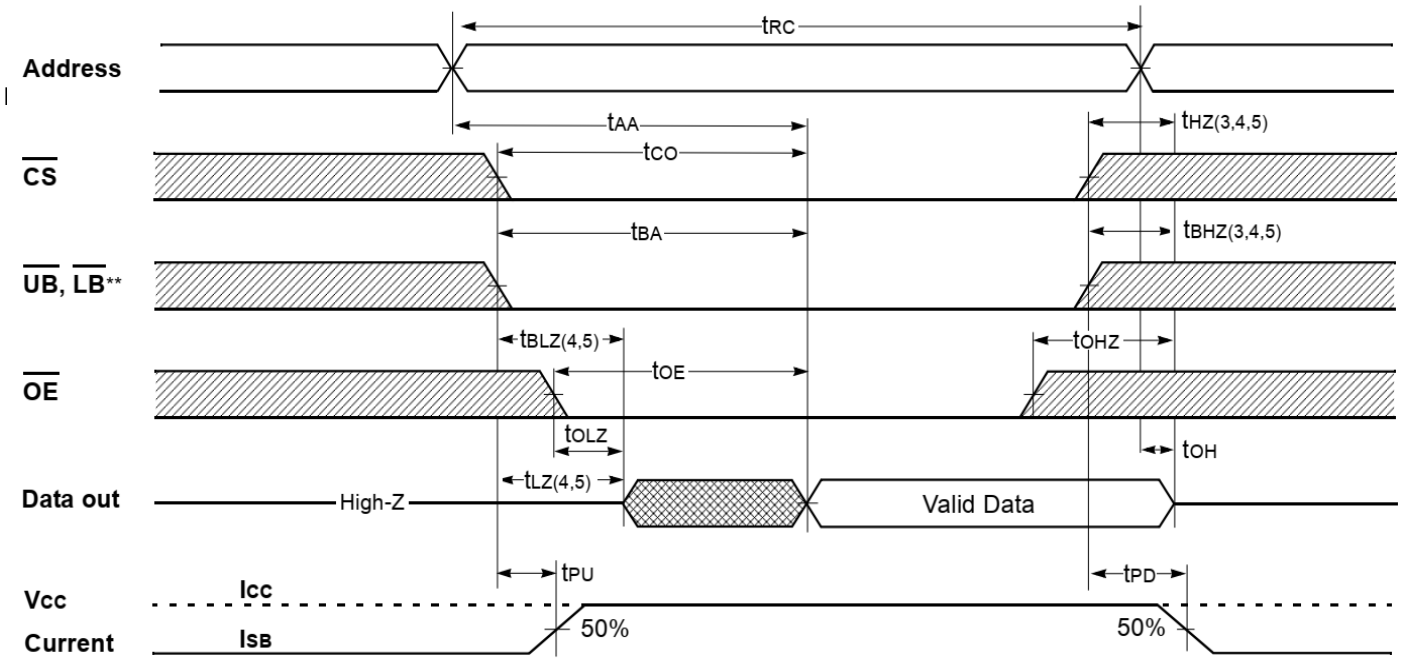
Timing Diagrams

Timing Waveform of Read Cycle(1) (Address Controlled, $\overline{CS}$ =$\overline{OE}$ =VIL, $\overline{WE}$ =VIH, $\overline{UB}$, $\overline{LB}$ =VIL [1])



Notes:
1. Those parameters are applied for x16 mode only.

Timing Waveform of Read Cycle(2) ($\overline{WE}$ = VIH)

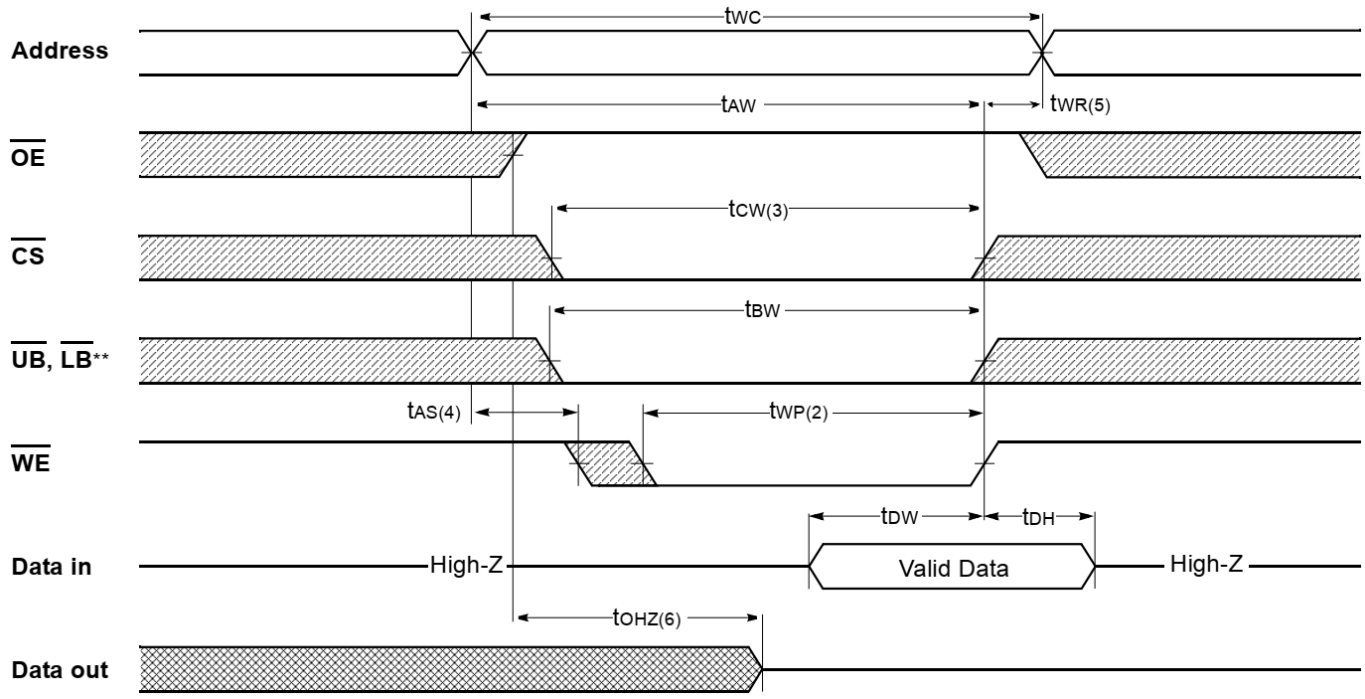


Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common DQ applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

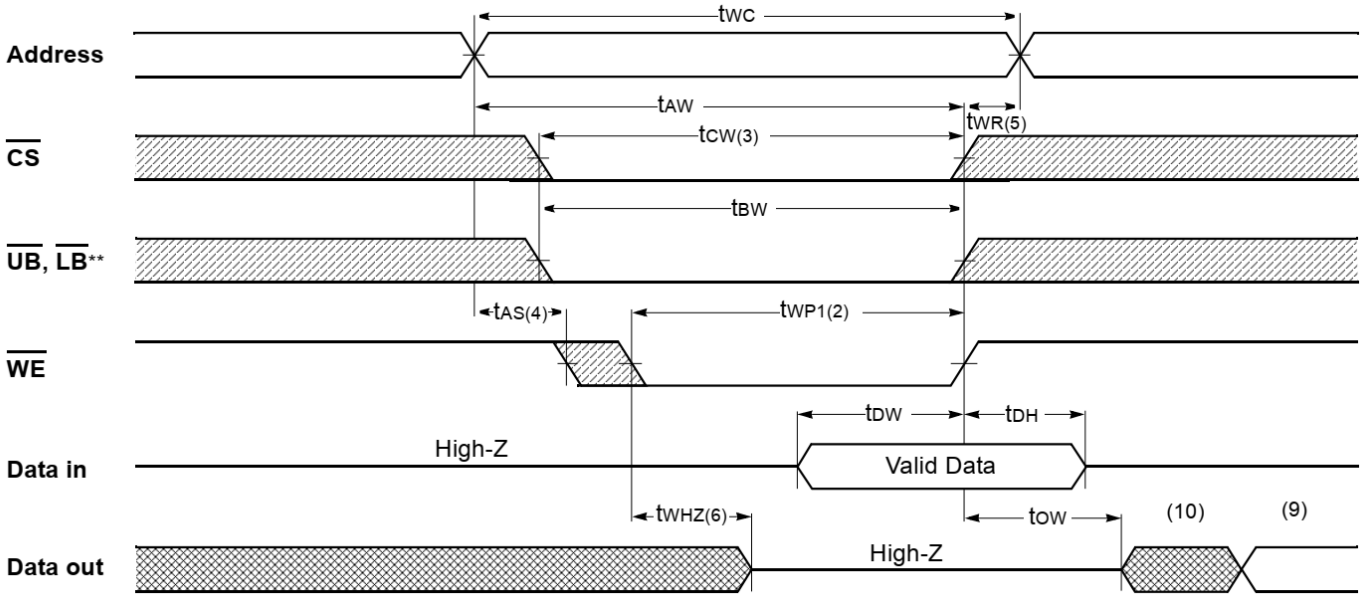
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(1) ($\overline{OE}$ Clock)



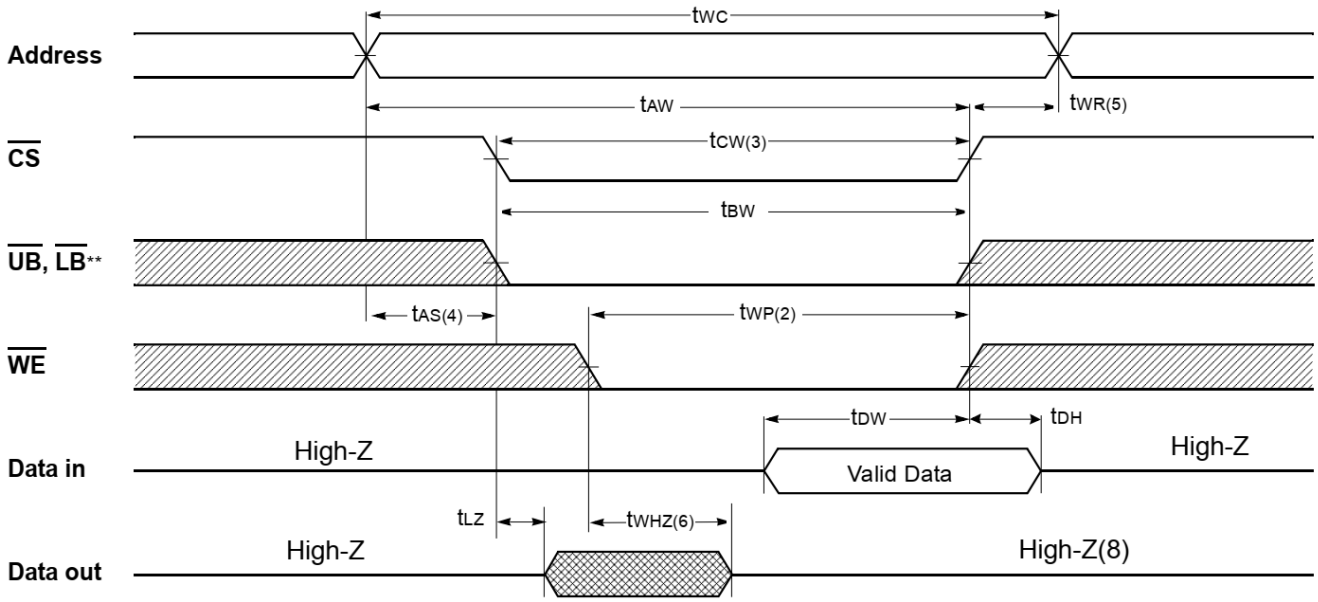
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(2) ($\overline{OE}$ = Low Fix)



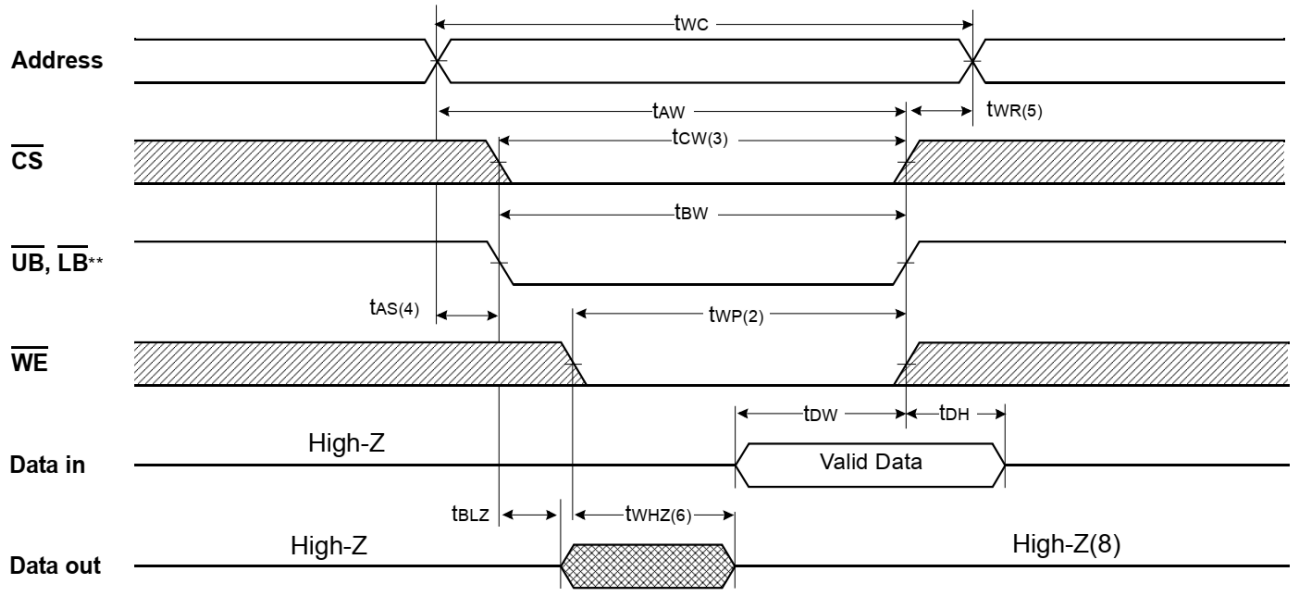
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(3) ($\overline{CS}$ Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



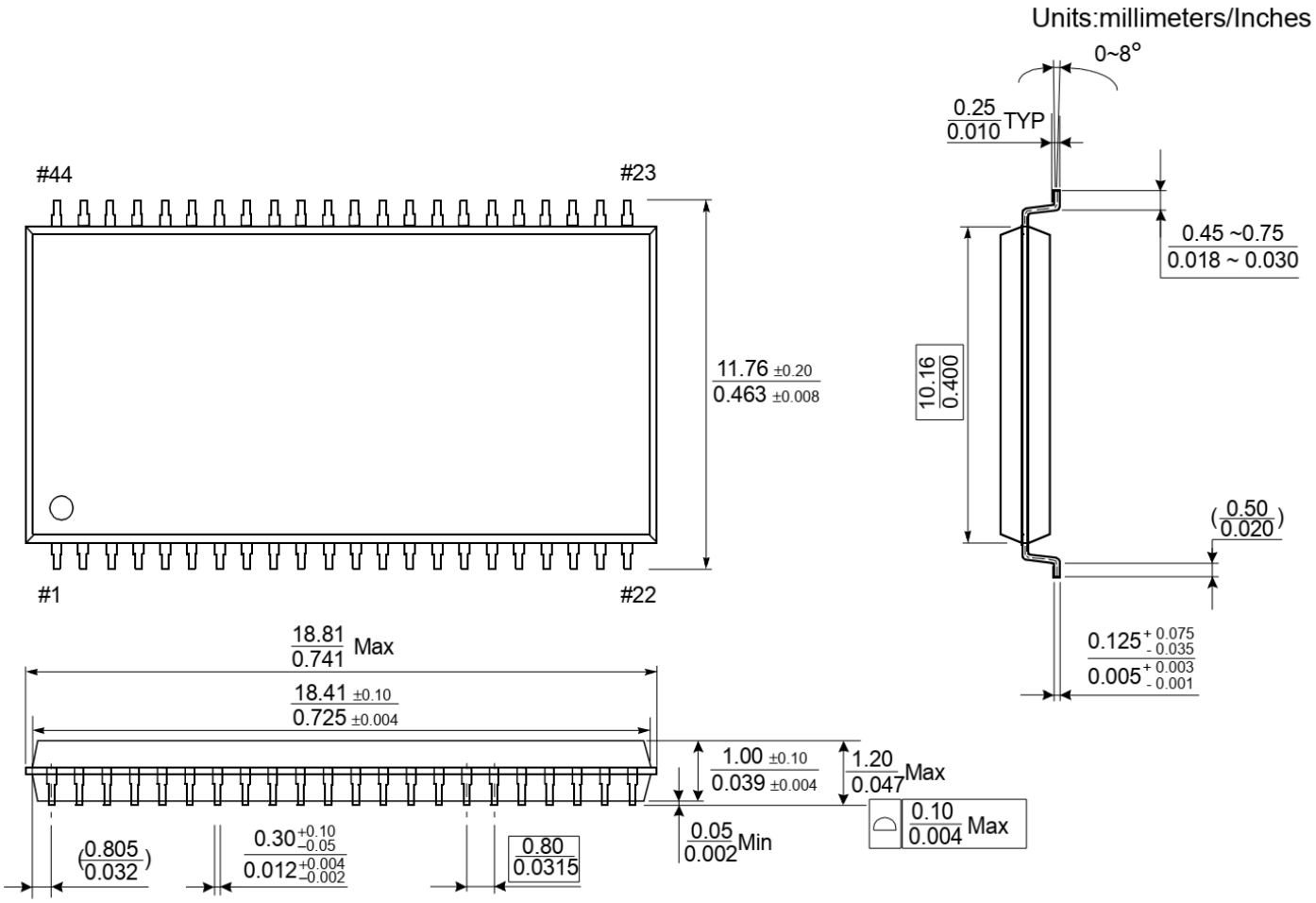
Notes (Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or WE going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not . be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$, goes low simultaneously with $\overline{WE}$ going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only.

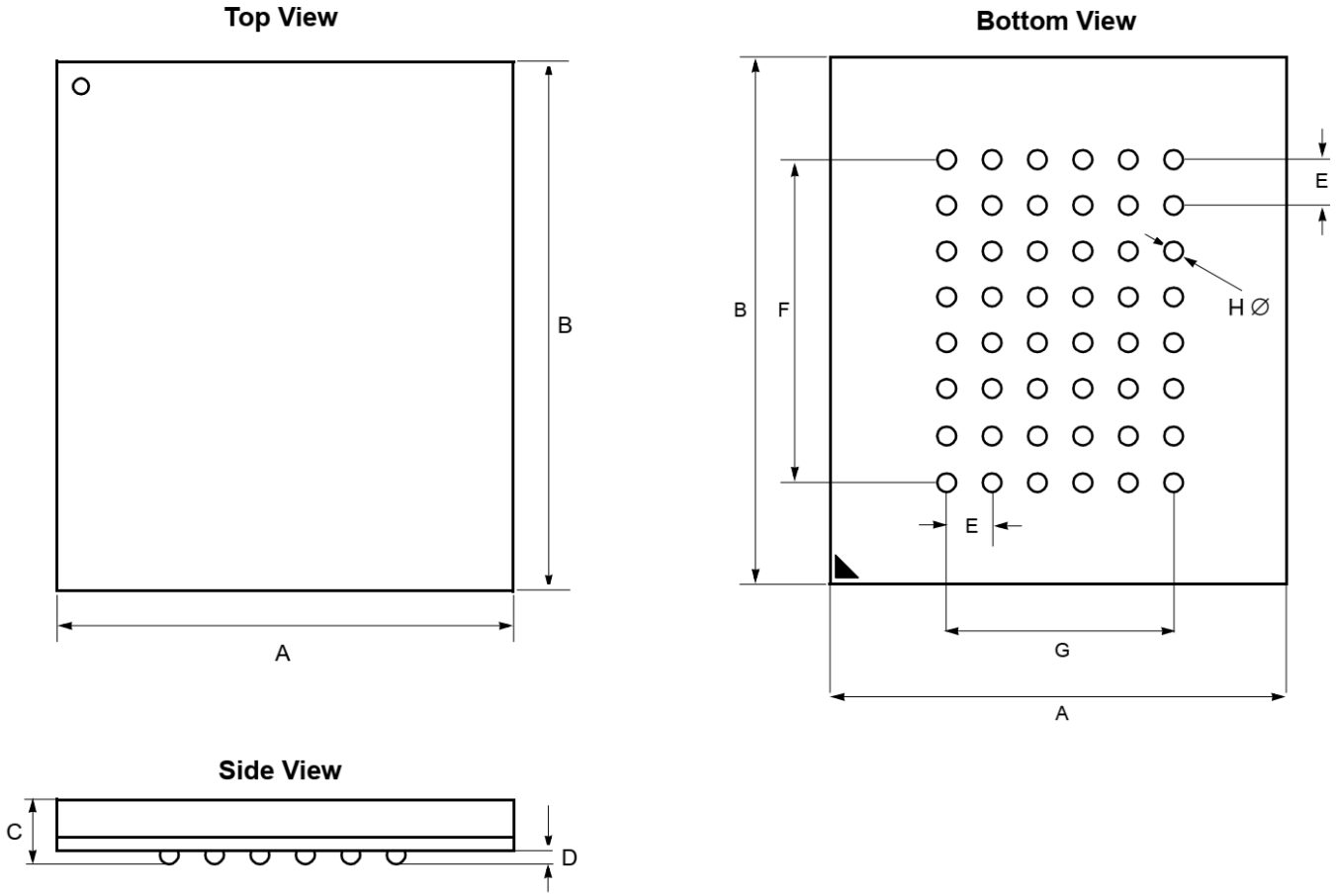
Package Dimensions

44-TSOP2-400BF



48FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array



Symbol	Value	Units	Note		Symbol	Value	Units	Note
A	6 ± 0.1	mm			**E**	0.75	mm	
B	8 ± 0.1	mm			**F**	5.25	mm	
C	1.1 ± 0.1	mm			**G**	3.75	mm	
D	0.25 ± 0.05	mm			**H**	0.35 ± 0.05	mm	

Revision History

Revision	Data	Description
0.0	Aug. 2023	Initial Release, Preliminary

* Products and specifications discussed herein are subject to change by Netsol without notice.