32Mb SPI MRAM M-die

Single/Dual/Quad IO SPI MRAM

1.8V

- **S3A3204R3M**

Datasheet

Feature

- Supports Serial Peripheral Interface with Mode 0 and Mode 3
  - Single SPI (1-1-1, 1-1-2, 1-2-2, 1-1-4, 1-4-4)
  - Dual SPI (2-2-2)
  - Quad SPI (4-4-4)
- Operating Frequency
  - Single Data Rates (SDR) : 133MHz
  - Double Data Rates (DDR) : 67MHz
- Supports XIP for read and write operations
- Fast write time and single byte writable
- Data protection
  - $\overline{WP}$ pin write protection
  - Block lock protection
- Nonvolatile status and configuration registers
- Identification
  - 64-bit unique ID
  - 64-bit serial number - user writable
- Augmented 512-byte nonvolatile-area
  - Read and write with user-protection
- Deep power down for low-power
- Supports JEDEC reset
- Memory cell : STT-MRAM
- Density
  - 32Mb
- Data Integrity : No external ECC required
- Data Endurance
  - Unlimited read cycle
  - 10^{14} write cycles
- Data Retention
  - 20 years at 85°C
- Single Power Supply Operation
  - S3A3204R3M: 1.71V~1.98V
- Operating Temperature Range
  - Industrial Temperature : -40°C to 85°C
- RoHS compliant packages
  - 8pad WSON (5.0mm x 6.0mm)
  - 8pin SOIC (150mil)

Performance

Operation	Typical Values	Units
	1.8V(S3A3204R3M)	
Frequency(SDR)	133 (Max.)	MHz
Frequency(DDR)	67 (Max.)	MHz
Standby Current	560	µA
Deep Power Down Current	60	µA
Active Read Current (4-4-4) SDR @133MHz	10	mA
Active Write Current (4-4-4) SDR @133MHz	25	mA

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General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM).
It features a SPI bus interface, XIP(execute-in-place) functionality and hardware/software based data protection mechanisms.
SPI (Serial Peripheral Interface) is a synchronous serial communication interface with command, address and data signals.

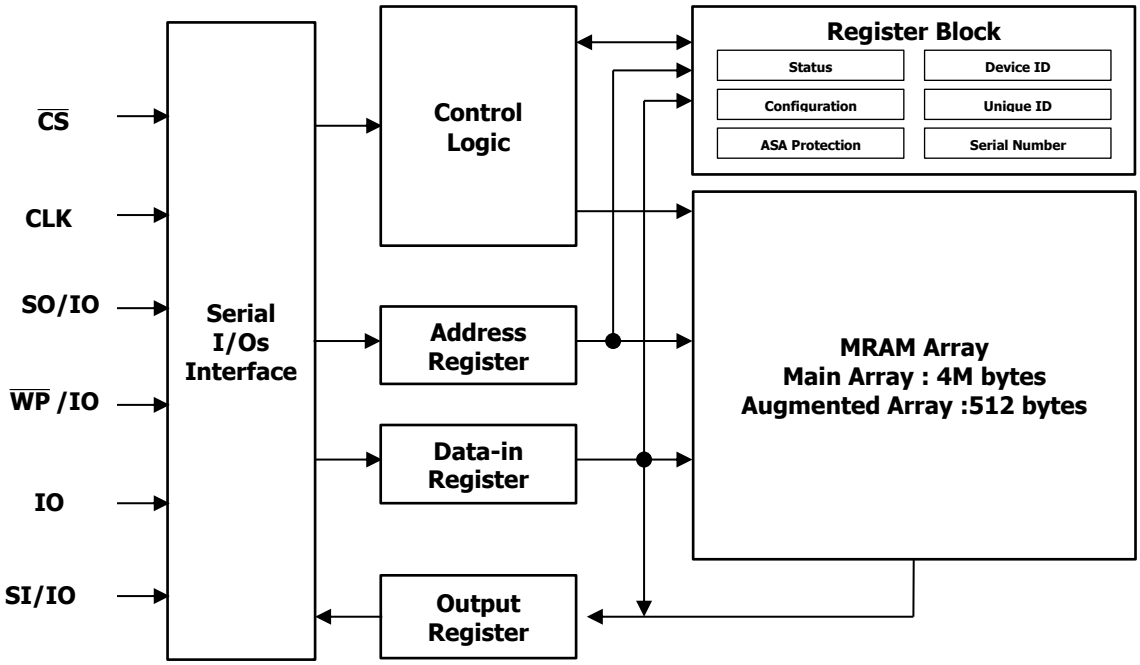
It requires less pin counts than parallel interface and is easy to be configured on the system.
The device can replace Flash, FeRAM or (nv)SRAM with same functionality and non-volatility.

The device provides various SPI modes to allow options for bandwidth expansion.
SSPI (Single SPI) modes has single(1) pin for command signals.
And user can select an option for how many pin to be allocated to address and data signals among 1 pin, 2 pins or 4 pins.
DSPI (Dual SPI) modes provides dual(2) pins for command, address and data signals.
QSPI (Quad SPI) modes provides quad(4) pins for command, address and data signals.

The device has nonvolatile register bits – status register, configuration register, serial number register, augmented 512 bytes and protection register for augmented bytes. These register bits are required to be set at least once on power-up after high temperature solder reflow process.

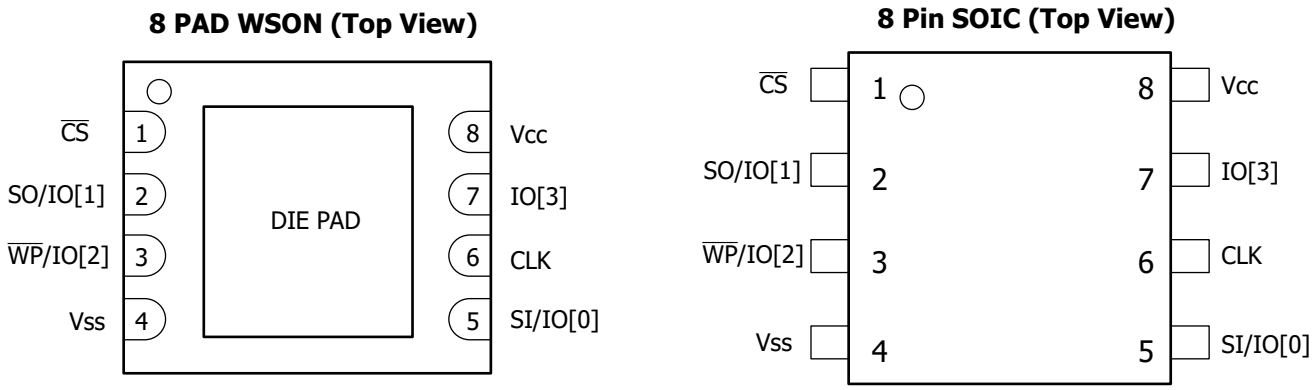
The device is available in small footprint 8-pad WSON and 8-pin SOIC packages.
These packages are compatible with similar low-power volatile and non-volatile products.
The device is offered with industrial (-40°C to 85°C) operating temperature range.

Figure 1 : Functional Block Diagram



Package Pin Configuration

Figure 2 : Pinout



Pin Description

Table 1 : Pin Description

Pin	Type	Description
$\overline{CS}$	Input	**Chip Select:** When $\overline{CS}$ is driven Low, read or write operation are initiated. When $\overline{CS}$ is driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. $\overline{CS}$ should be High at power-up to prevent abnormal write operation. This pin does not have internal pullup resistor.
CLK	Input	**Clock**: In SDR(single data rate) mode, command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In DDR(double data rate) mode command is latched on the rising edge of the clock and address and data inputs are latched on the rising and falling edges of the clock. Similarly, Data is output on both edges of the clock. The two SPI clock modes are supported as follows. • SPI Mode 0 : SDR and DDR • SPI Mode 3 : SDR only
$\overline{WP}$/IO[2]	Input /Bidirectional	**Write Protect (SSPI/DSPI):** Write protects the status register in conjunction with the WREN bit (SR[1]) of the status register. The writing of status register is protected in related with $\overline{WP}$ and WPEN. See "Table 13 : Write Protection Modes". This pin does not have internal pullups, it cannot be left floating and must be driven. $\overline{WP}$ is valid in Single SPI and Dual SPI mode. **IO[2] :** The bidirectional I/O in Quad SPI mode.
IO[3]	Bidirectional	**IO[3] :** The bidirectional I/O in Quad SPI modes.
SI/IO[0]	Input /Bidirectional	**SI :** The serial input in Single SPI mode. **IO[0] :** The bidirectional I/O in Dual and Quad SPI modes
SO/IO[1]	Output /Bidirectional	**SO :** The serial data output in Single SPI mode. **IO[1] :** The bidirectional in Dual and Quad SPI modes.
Vcc	Supply	Power pin
Vss	Supply	Ground pin
DIE PAD	-	DIE PAD on the bottom of WSON package should be connected to VSS or floating.

Power On/Off Sequence : 1.8V Device

- When power-up, power-down or power-loss, $\overline{CS}$ must follow Vcc to provide data protection.
- It is recommended that $\overline{CS}$ must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
- A 10KΩ pull-up resistor between Vcc and $\overline{CS}$ pin is recommended.
- Software reset operation is required after t_{PU}.
- Normal operation must start after t_{SRST}.

Figure 3 : Power-up/down Behavior : 1.8V Device

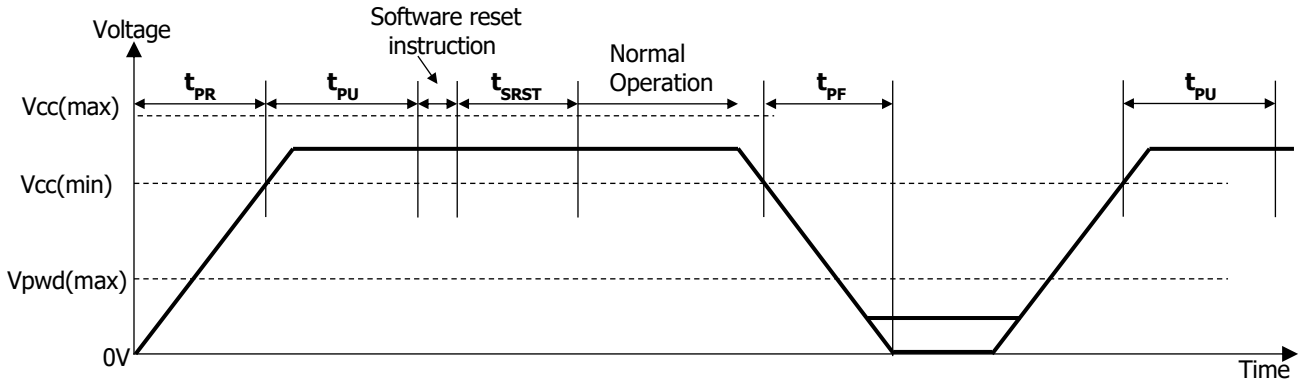


Table 2 : Power Up/Down Timing – 1.8V Device

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	1.71	1.98	V
Vcc rising time	t_{PR} (1)	30	-	µs/V
Vcc falling time	t_{PF}(1)	30	-	µs/V
Vcc(min) to $\overline{CS}$ Low (first instruction) time	t_{PU}(1)	2.0	-	ms
Vcc needed to below Vpwd for ensuring initialization will occur	V_{PWD}(1)	-	0.8	V
Software Reset Time	t_{SRST}(1)	2.0	-	ms

Notes:
1: These parameters are guaranteed by characterization; not tested in production.

Memory Organization

Memory Map

Table 3 : Memory Map

Density	Address Range	24-bit Address [23:0]	
32Mb	000000h – 3FFFFFh	[23:22] – Logic '0'	[21:0] – Addressable

Augmented 512-Byte Area Map

Table 4 : Augmented 512-Byte Area Map

Density	Address Range	24-bit Address [23:0]	
32Mb	000000h – 0001FFh[1]	[23:9] – Logic '0'	[8:0] - Addressable

Notes:
1: The augmented 512-byte area is divided into 8 individually readable and writeable sections (64 bytes per section). After an individual section is written, it can be write protected for each section to prevent further writing.

Register Address Map

The device provides the register read/write instructions to read and write data of each register. In addition, the device provides the register read and/or write function based on addresses by RDAR(65h) and WRAR(71h) commands.

Table 5 : Register Address

Register Name	Address
Status Register	0x000000h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Configuration Register 3	0x000004h
Configuration Register 4	0x000005h
Device Identification Register	0x000030h
Unique Identification Register	0x000040h
Serial Number Register	0x000080h

Notes:
1: Register address space is different from the memory array and augmented 512-byte area.

Instruction Command Set

Table 6 : Control Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
No operation	NOOP	00	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Write Enable	WREN	06	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Write Disable	WRDI	04	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Enable DSPI	DPIE	37	1-0-0, 4-0-0		SDR			133Mhz
Enable QSPI	QPIE	38	1-0-0, 2-0-0		SDR			133Mhz
Enable SSPI	SPIE	FF	2-0-0, 4-0-0		SDR			133Mhz
Enter Deep Power Down	DPDE	B9	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Exit Deep Power Down	DPDX	AB	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Software Reset Enable	SRTE	66	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz
Software Reset*	SRST	99	1-0-0, 2-0-0, 4-0-0		SDR			133Mhz

Notes:
1: Software Reset (SRST) requires Software Reset Enable (SRTE) implemented in advance.
2: SSPI mode is enabled after power-on, software reset or JEDEC reset.

Table 7 : Read Register Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Status Register	RDSR	05	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Configuration Register 1	RDC1	35	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Configuration Register 2	RDC2	3F	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Configuration Register 3	RDC3	44	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Configuration Register 4	RDC4	45	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Configuration Register 1, 2, 3, 4	RDCX	46	1-0-1, 2-0-2, 4-0-4		SDR	4		133Mhz
Read Device ID	RDID	9F	1-0-1, 2-0-2, 4-0-4		SDR	4		133Mhz
Read Unique ID	RUID	4C	1-0-1, 2-0-2, 4-0-4		SDR	8		54MHz
Read Serial Number Register	RDSN	C3	1-0-1, 2-0-2, 4-0-4		SDR	8		133Mhz
Read Augmented 512-byte Protection Register	RDAP	14	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Read Any Register - Address Based	RDAR	65	1-1-1, 2-2-2, 4-4-4		SDR	1,4,8	O	133Mhz

Notes:
1. Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

Table 8 : Write Register Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Write Status Register	WRSR	01	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Write Configuration Registers 1, 2, 3, 4	WRCX	87	1-0-1, 2-0-2, 4-0-4		SDR	4		133Mhz
Write Serial Number Register	WRSN	C2	1-0-1, 2-0-2, 4-0-4		SDR	8		133Mhz
Write Augmented 512-byte Protection Register	WRAP	1A	1-0-1, 2-0-2, 4-0-4		SDR	1		133Mhz
Write Any Register - Address Based	WRAR	71	1-1-1, 2-2-2, 4-4-4		SDR	1,8		133Mhz

Notes:
1. Write Enable (WREN) should be implemented in advance of Write Register Instruction set regardless of CR4[1:0] setting.
2. The WREN prerequisite for write operation of memory array and augmented 512-byte area is described in Configuration Register 4.

Table 9 : Read Memory Array Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Memory Array - SDR	READ	03	1-1-1		SDR	1→∞		54MHz
Fast Read Memory Array - SDR	RDFT	0B	1-1-1, 2-2-2, 4-4-4	O	SDR	1→∞	O	133Mhz
Fast Read Memory Array - DDR	DRFR	0D	1-1-1, 2-2-2, 4-4-4	O	DDR	1→∞	O	67MHz
Read Dual Output Memory Array - SDR	RDDO	3B	1-1-2, 2-2-2	O	SDR	1→∞	O	133Mhz
Read Dual Output Memory Array - DDR	DRDO	3D	1-1-2, 2-2-2	O	DDR	1→∞	O	67MHz
Read Quad Output Memory Array - SDR	RDQO	6B	1-1-4, 4-4-4	O	SDR	1→∞	O	133Mhz
Read Quad Output Memory Array – DDR	DRQO	6D	1-1-4, 4-4-4	O	DDR	1→∞	O	67MHz
Read Dual I/O Memory Read - SDR	RDDI	BB	1-2-2, 2-2-2	O	SDR	1→∞	O	133Mhz
Read Dual I/O Memory Read - DDR	DRDI	BD	1-2-2, 2-2-2	O	DDR	1→∞	O	67MHz
Read Quad I/O Memory Read - SDR	RDQI	EB	1-4-4, 4-4-4	O	SDR	1→∞	O	133Mhz
Read Quad I/O Memory Read - DDR	DRQI	ED	1-4-4, 4-4-4	O	DDR	1→∞	O	67MHz

Notes:
1: Read Instruction must include Latency cycles to meet operating frequency.
2: Latency is configurable through Configuration Register 2 (CR2[3:0]) and frequency dependent. Required latency is described in Configuration Register 2.

Table 10 : Write Memory Array Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Write Memory Array - SDR	WRTE	02	1-1-1, 2-2-2, 4-4-4		SDR	1→∞		133Mhz
Fast Write Memory Array - SDR	WRFT	DA	1-1-1, 2-2-2, 4-4-4	O	SDR	1→∞		133Mhz
Fast Write Memory Array - DDR	DRFW	DE	1-1-1, 2-2-2, 4-4-4	O	DDR	1→∞		67MHz
Write Dual Input Memory Array - SDR	WDUI	A2	1-1-2(1), 2-2-2	O	SDR	1→∞		133Mhz
Write Dual Input Memory Array – DDR	DWUI	A4	1-1-2(2), 2-2-2	O	DDR	1→∞		67MHz
Write Quad Input Memory Array - SDR	WQDI	32	1-1-4(1), 4-4-4	O	SDR	1→∞		133Mhz
Write Quad Input Memory Array - DDR	DWQI	31	1-1-4(2), 4-4-4	O	DDR	1→∞		67MHz
Write Dual I/O Memory Array - SDR	WDIO	A1	1-2-2, 2-2-2	O	SDR	1→∞		133Mhz
Write Dual I/O Memory Array - DDR	DWIO	A3	1-2-2, 2-2-2	O	DDR	1→∞		67MHz
Write Quad I/O Memory Array - SDR	WQIO	D2	1-4-4, 4-4-4	O	SDR	1→∞		133Mhz
Write Quad I/O Memory Array - DDR	DWQO	D1	1-4-4, 4-4-4	O	DDR	1→∞		67MHz

Notes:
1: Write Enable (WREN) for array writing is configurable (Configuration Register 4 – CR4[1:0])
(1) limited to 120MHz
(2) limited to 60MHz

Table 11 : Augmented 512-Byte Area Instruction Set

Instruction Name	Command	Opcode (Hex)	Interface Type (CMD-ADDR-Data)	XIP	Data Rate	Data Bytes	Latency Cycles	Max. Frequency
Read Augmented 512-Byte Area - SDR	RDAS	4B	1-1-1		SDR	1→ 512	O	133Mhz
Write Augmented 512-Byte Area - SDR	WRAS	42	1-1-1		SDR	1→ 512		133Mhz

Notes:
1: The address bits ADDR[23:9] must be Logic '0' for this Instruction.
2: Write Enable (WREN) for array writing is configurable (Configuration Register 4 – CR4[1:0])

Register Description

The device has nonvolatile register bits – status register, configuration register, serial number register, augmented 512-byte area and protection register for augmented 512-byte area. These register bits are required to be set at least once on power-up after high temperature solder reflow process.

Status Register / Device Protection Register

The device offers both hardware and software based data protection schemes. Hardware protection is through $\overline{WP}$ pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array. Status Register contains options for enabling/disabling data protection.
By controlling configuration bits in Status Register, user can protect data in memory array based on software protection schemes.

Table 12 : Status Register-Data Protection

Bits	Name	Read/ Write	Default State	Description
SR[7]	WPEN	R/W	-	Hardware Based $\overline{WP}$ Protect Bit 1: Protection Enabled – write protects when $\overline{WP}$ is Low 0: Protection Disabled – Doesn't write protect when $\overline{WP}$ is Low
SR[6]	SNPEN	R/W	-	Serial Number Protect Bit 1: Serial Number Write protected 0: Serial Number Writable
SR[5]	TB	R/W	-	Top/Bottom Memory Array Protect Selection 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BP[2]	R/W	-	Block Protection Bits
SR[3]	BP[1]	R/W	-	
SR[2]	BP[0]	R/W	-	
SR[1]	WREN	R	0	Write Protection Enable 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	R	-	Reserved for future use

Notes: SR[7:2] are nonvolatile bits.

Write Protection Modes

WPEN bit (SR[7]) is used in conjunction with the WREN bit (SR[1]) and the $\overline{WP}$ pin to provide hardware block protection. SR[7:2] will remain set from the nonvolatile registers whenever the power is on. The WREN bit is volatile and set "1" by the Write Enable command. It is set to "0" at power up. The device enters hardware protection when the $\overline{WP}$ input is low and the Status Register WPEN bit is set to 1, and the status and configuration register bits can not be changed.
The device exits from hardware protection when the $\overline{WP}$ pin goes high or WPEN bit is set to 0, and the register bits can be changed.

Table 13 : Write Protection Modes

WREN	WPEN	$\overline{WP}$ (Pin)	Status & Configuration Registers	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	0	Protected	Protected	Unprotected
1	1	1	Unprotected	Protected	Unprotected

Notes:
1: Memory address range protection based on Block Protection Bits
2. X: Don't Care – Can be Logic '0' or '1'
3. Protected: Write protected, Unprotected: Writable

Block Protection Modes

The write protection blocks for the memory array are determined by the status register bits (TB and BP[2:0]) as Table 14. TB and BP[2:0] can be modified by WRSR command when the $\overline{WP}$ input is high or the Status Register WPEN bit is set to 0, and MAPLK(CR1[2]) is set to 0.

Table 14 : Block Protection Address Range Selection

TB	BP[2]	BP[1]	BP[0]	Protected Portion	32Mb
0/1	0	0	0	None	None
0	0	0	1	Upper 1/64	3F0000h – 3FFFFFh
0	0	1	0	Upper 1/32	3E0000h – 3FFFFFh
0	0	1	1	Upper 1/16	3C0000h – 3FFFFFh
0	1	0	0	Upper 1/8	380000h – 3FFFFFh
0	1	0	1	Upper 1/4	300000h – 3FFFFFh
0	1	1	0	Upper 1/2	200000h – 3FFFFFh
1	0	0	1	Lower 1/64	000000h – 00FFFFh
1	0	1	0	Lower 1/32	000000h – 01FFFFh
1	0	1	1	Lower 1/16	000000h – 03FFFFh
1	1	0	0	Lower 1/8	000000h – 07FFFFh
1	1	0	1	Lower 1/4	000000h – 0FFFFFh
1	1	1	0	Lower 1/2	000000h – 1FFFFFh
0/1	1	1	1	All	000000h – 3FFFFFh

Augmented 512-Byte Area Protection

Augmented 512-Byte Area Protection register contains options for enabling/disabling data protection for eight 64-byte sections.

Table 15 : Augmented 512-Byte Area Protection Register – Read and Write

Bits	Name	Address Range	Read/ Write	Default State	Description
ASP[7]	ASPS[7]	0001C0h – 0001FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	000180h – 0001BFh	R/W	0	
ASP[5]	ASPS[5]	000140h – 00017Fh	R/W	0	
ASP[4]	ASPS[4]	000100h – 00013Fh	R/W	0	
ASP[3]	ASPS[3]	0000C0h – 0000FFh	R/W	0	
ASP[2]	ASPS[2]	000080h – 0000BFh	R/W	0	
ASP[1]	ASPS[1]	000040h – 00007Fh	R/W	0	
ASP[0]	ASPS[0]	000000h – 00003Fh	R/W	0	

Notes : ASP[7:0] are nonvolatile bits.

Configuration Register 1 (Read/Write)

Configuration Register 1 controls locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register.

Table 16 : Configuration Register 1 – Read and Write

Bits	Name	Read/ Write	Default State	Selection Options
CR1[7]	RSVD	R/W	-	Reserved for future use
CR1[6]	RSVD	R/W	-	Reserved for future use
CR1[5]	RSVD	R/W	-	Reserved for future use
CR1[4]	RSVD	R/W	-	Reserved for future use
CR1[3]	RSVD	R/W	-	Reserved for future use
CR1[2]	MAPLK	R/W	-	Status Register TB, BP[2:0] Protect 1: Lock TB and BP[2:0] 0: Unlock TB and BP[2:0]
CR1[1]	RSVD	R/W	-	Reserved for future use
CR1[0]	ASPLK	R/W	-	Augmented 512-Byte Area Data Protection 1: Write Protection for Augmented Area Data regardless of ASP[7:0] 0: Write Protection for Augmented Area Data depending on ASP[7:0]

Notes : CR1[7:0] are nonvolatile bits.

Configuration Register 2 (Read/Write)

Configuration Register 2 controls the interface type along with memory array access latency.

Table 17 : Configuration Register 2 – Read and Write

Bits	Name	Read/ Write	Default State	Description
CR2[7]	RSVD	R/W	-	Reserved for future use
CR2[6]	QPIEN	R	0	Quad SPI (QPI 4-4-4) Interface Mode 1: Quad SPI (QPI 4-4-4) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[5]	RSVD	R/W	0	It must be written as 0
CR2[4]	DPIEN	R	0	Dual SPI (DPI 2-2-2) Interface Mode 1: Dual SPI (DPI 2-2-2) Enabled 0: Single SPI (SPI 1-X-X) Enabled
CR2[3]	RL[3]	R/W	-	Read Latency Selection Bits : CR2[3:0] 0000: 0 Cycle 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	RL[2]		-	
CR2[1]	RL[1]		-	
CR2[0]	RL[0]		-	

Notes:
1. Read Latency is frequency dependent.
2. Read(03h) does not depend on Read latency Selection Bits, CR2[3:0].
3. CR2[7,5,3:0] are nonvolatile bits.
4. CR2[5] must be written as 0

Table 18 : Read Latency Cycles vs. Maximum Frequency (Memory Area)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (READ 03h)	SDR	-	0	54MHz
1-1-1	SDR	O	2-15	133MHz (120MHz)
1-1-2, 1-2-2, 2-2-2			7-15	
1-1-4, 1-4-4, 4-4-4			9-15	
1-1-1	DDR		2-15	67MHz (60MHz)
1-1-2, 1-2-2, 2-2-2			7-15	
1-1-4, 1-4-4, 4-4-4			9-15	

Notes:
1. Read(03h) does not depend on Read latency Selection Bits, CR2[3:0]. The latency of Read(03h) is always 0-cycle.

Table 19 : Read Latency Cycles vs. Maximum Frequency (Augmented 512-Byte Area)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (RDAS 4Bh)	SDR	-	7-15	67MHz
1-1-1 (RDAS 4Bh)	SDR	-	9-15	133MHz

Table 20 : Latency Cycles vs. Maximum Frequency (Read Any Register Instruction)

Read Type	Data Rate	XIP	Latency Cycles	Max Frequency
1-1-1 (RDAR 65h)	SDR	-	8	133MHz
2-2-2 (RDAR 65h)	SDR	-	4	133MHz
4-4-4 (RDAR 65h)	SDR	-	2	133MHz

Notes:
1. RDAR(65h, read any register instruction) does not depend on Read latency Selection Bits, CR2[3:0].

Configuration Register 3 (Read/Write)

Configuration Register 3 controls the output driver strength along with the boundary size of read data wrapping.

Table 21 : Configuration Register 3 – Read and Write

Bits	Name	Read/ Write	Description
CR3[7]	DRV[2]	R/W	Output Driver Strength Selection DRV[2:0] 1.8V 000: 35Ω 001: 95Ω 010: 63Ω 011: 50Ω 100: 40Ω 101: 30Ω 110: 26Ω 111: 22Ω
CR3[6]	DRV[1]		
CR3[5]	DRV[0]		
CR3[4]	WRPEN	R/W	Read WRAP Enable 1: Read Wrap Enabled 0: Read Wrap Disabled
CR3[3]	RSVD	R/W	Reserved for future use
CR3[2]	WRPL[2]	R/W	Wrap length configuration WRPL[2:0] 000: 16-byte wrap 001: 32-byte wrap 010: 64-byte wrap 011: 128-byte wrap 100: 256-byte wrap 101: 512-byte wrap 110: 1K-byte wrap 111: Reserved
CR3[1]	WRPL[1]		
CR3[0]	WRPL[0]		

Notes:
1. Default output strength is DRV[2:0]=000.
2. CR3[7:0] are nonvolatile bits.

	Description
WRPEN(CR3[4]) =Low	Read and write operation : continuous mode Read or write operation starts at the input address, and once the address reaches the maximum address boundary, it automatically returns to minimum address(000000h) until $\overline{CS}$ goes to high.
WRPEN(CR3[4]) =High	Read operations : wrap mode Read wrap mode is enabled when WRPEN(CR3[4]) is High, and the read data wrap length is controlled by WRPL[2:0]. The output data starts at the input address, data are output sequentially. Once it reaches the ending boundary, the output will wrap around to the beginning boundary automatically until $\overline{CS}$ is pulled high. Write operation : continuous mode Write operation starts at the input address, and once the address reaches the maximum address boundary, it automatically returns to minimum address(000000h) until $\overline{CS}$ goes to high.

Configuration Register 4 (Read/Write)

Configuration Register 4 controls Write Enable protection (WREN – Status Register) reset functionality during memory array writing.
This functionality makes SPI MRAM compatible to other SPI devices.

Table 22 : Configuration Register 4 – Read and Write

Bits	Name	Read/ Write	Default State	Selection Options
CR4[7:2]	RSVD	R/W	-	Reserved for future use
CR4[1]	WRENS[1]		-	00: Normal: WREN is prerequisite to all Memory Array and Augmented 512-byte Area Write instruction. (WREN is reset after $\overline{CS}$ goes High) 01: SRAM: WREN is not a prerequisite to Memory Array and Augmented 512-byte Area Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write or Augmented 512-byte Area instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset after $\overline{CS}$ goes High) 11: Reserved
CR4[0]	WRENS[0]		-	

Notes:
1. Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write Instructions require WREN to be set and WREN resets once $\overline{CS}$ goes High for the write instruction.
   CR4[1:0] only affects the writing for memory and augmented 512-bytes area.
2. CR4[7:0] are nonvolatile bits.

Device Identification Register (Read Only)

Device identification register contains Netsol's Manufacturing ID along with device configuration information.

Table 23 : Device Identification Register – Read Only

Bits	Manufacturer ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temperature	Density	Reserved
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Reserved
31-24	23-20	19-16	15-12	11-8	7-0
1101 1001	0000 : QSPI	0010 : 1.8V	0000 : -40ºC~85ºC	0110 : 32Mb	00000001

Serial Number Register (Read/Write)

The device provides 64-bits Serial Number register and the user can write it.

Table 24 : Serial Number Register – Read and Write

Bits	Name	Description	Read/ Write	State
SN[63:0]	SN	Serial Number Value	R/W	User writable

Notes:
1: Serial Number Bits are nonvolatile and user should write the data after solder reflow process.

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 25 : Unique ID Register – Read Only

Bits	Name	Description	Read/ Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Device Operation

General Operation

Before an instruction is issued, status register should be checked to ensure device is ready for the intended operation.
When correct command is input to this device, it enters active mode and remains in active mode until next $\overline{CS}$ rising edge.

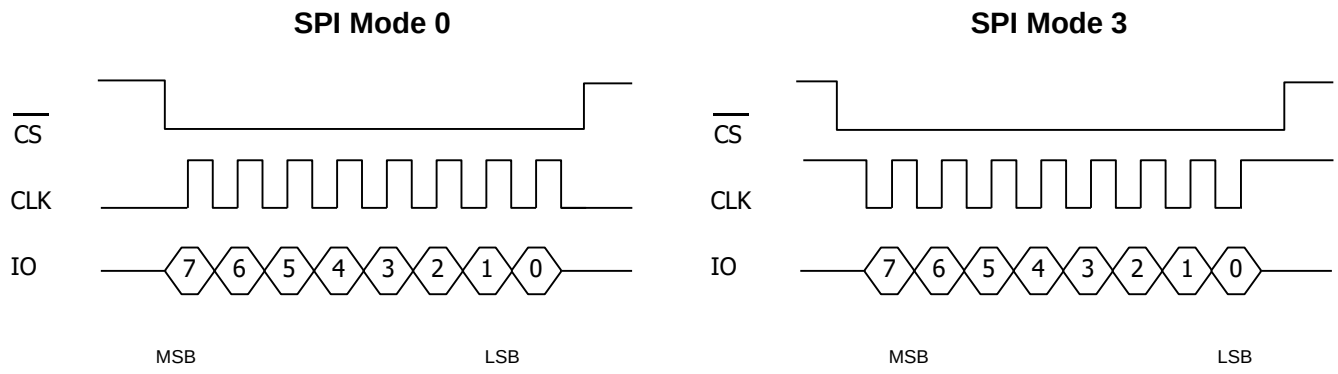
Do not enter an invalid opcode(except instruction set). When $\overline{CS}$ goes to high, the device enters standby mode.
All communication between a host and the device is in the form of commands. Commands define the operation that must be executed. Instruction consists of a command followed by an optional address modifier and data transferred.
All command, address and data information is transferred sequentially.

SPI Clock Modes

• The following two SPI clock modes are supported.

- SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR
- SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only

Figure 4 : SPI Clock Modes



Clock stays in low level during idle state and starts toggling by going high

Clock stays in high level during idle state and starts toggling by going low

SPI Interface Modes

• The device supports 3 categories of SPI interface modes.
- Single SPI (SSPI) : command is transferred through one I/O pin.
  1) Address and data are transferred through one pin
  2) Address is transferred through one pin, data is transferred through two pins
  3) Address is transferred through one pin, data is transferred through four pins
  4) Address and data are transferred through two pins
  5) Address and data are transferred through four pins

- Dual SPI (DSPI) : All command, address and data are transferred through two I/O pins.
- Quad SPI (QSPI) modes : All command, address and data are transferred through four I/O pins.

• Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document.
Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component.
As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

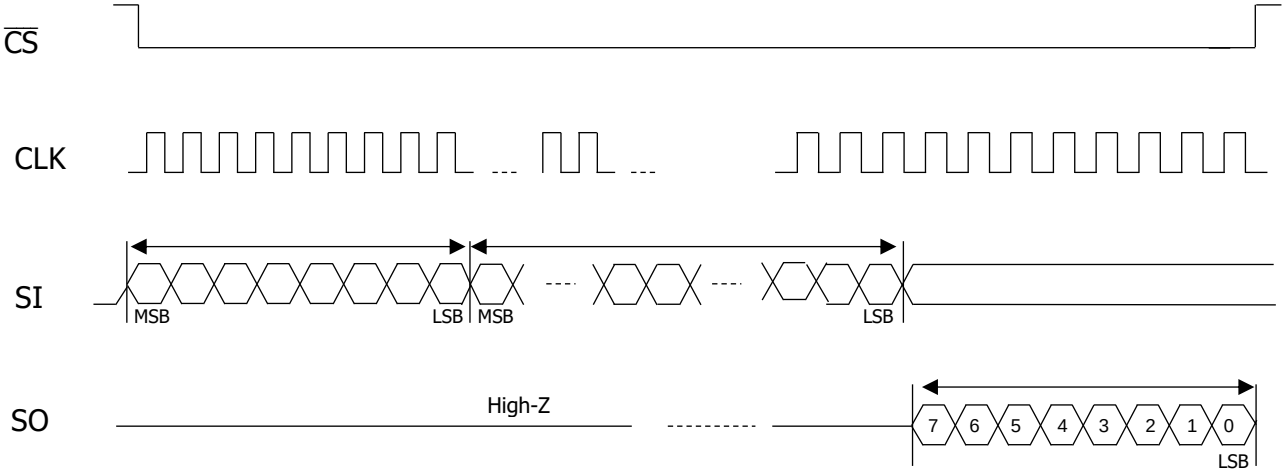
Table 26 : Pin Assignment / Interface Modes

Instruction Component	Interface Modes (Command-Address-Data)						
	SSPI 1-1-1	**SSPI 1-1-2**	**SSPI 1-2-2**	**DSPI 2-2-2**	**SSPI 1-1-4**	**SSPI 1-4-4**	**QSPI 4-4-4**
Command	SI/IO[0]	SI/IO[0]	SI/IO[0]	IO[1:0]	SI/IO[0]	SI/IO[0]	IO[3:0]
Address	SI/IO[0]	SI/IO[0]	IO[1:0]	IO[1:0]	SI/IO[0]	IO[3:0]	IO[3:0]
Data Input	SI/IO[0]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[3:0]
Data Output	SO/IO[1]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[3:0]

MSB/LSB Location in data bits

- The most significant bit(MSB) is placed first at all commands, address and data.

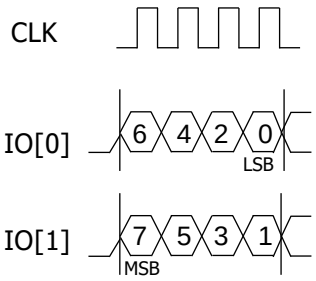
Figure 5 : Location of MSB and LSB



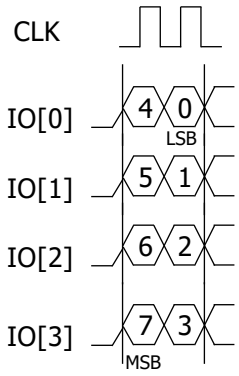
- For Dual SPI and Quad SPI, the order of data bits is alternately decided among the IO pins.

Figure 6 : MSB and LSB in DSPI and QSPI

1) Dual SPI



2) Quad SPI

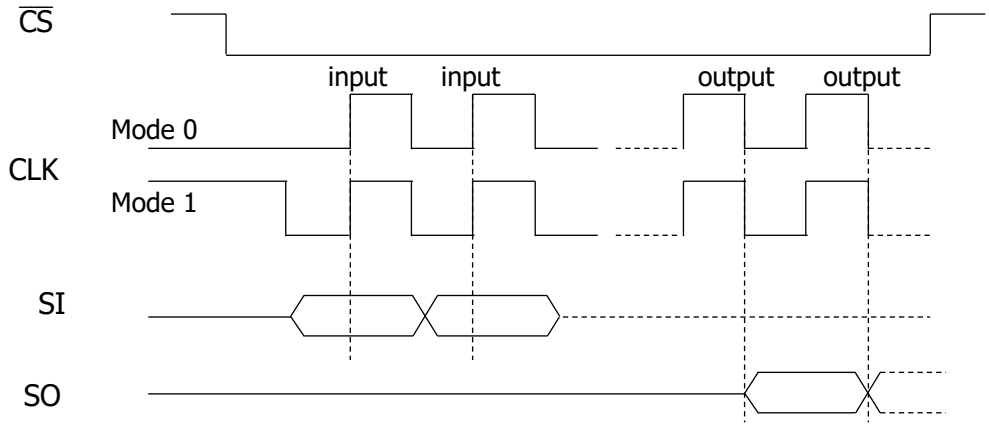


*** Notes;**
All commands, Address, XIP and Data follow this order

Data Rate (SDR/DDR)

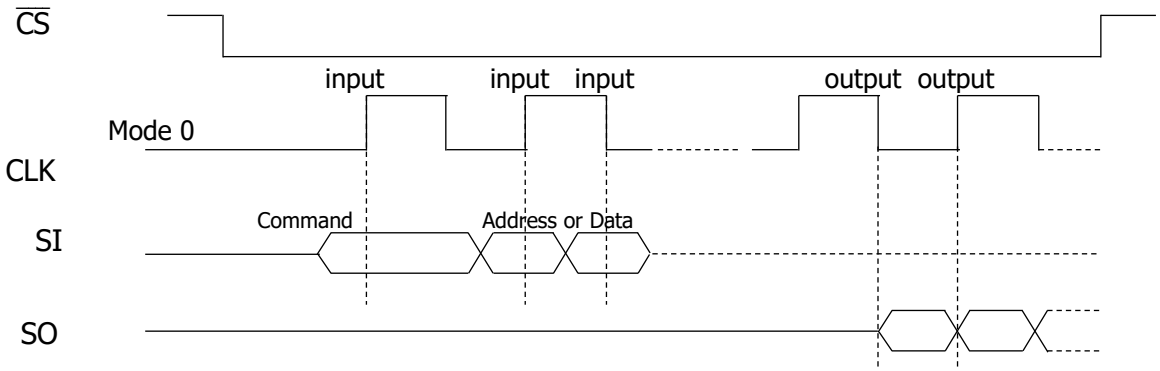
- In Single Data Rate mode (SDR), command, address and data inputs are latched on the rising edge of the clock. Data is outputted on the falling edge of the clock.

Figure 7 : Description of SDR Instruction Type



- In Double Data Rate mode (DDR), command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Data is output on both edges of the clock.

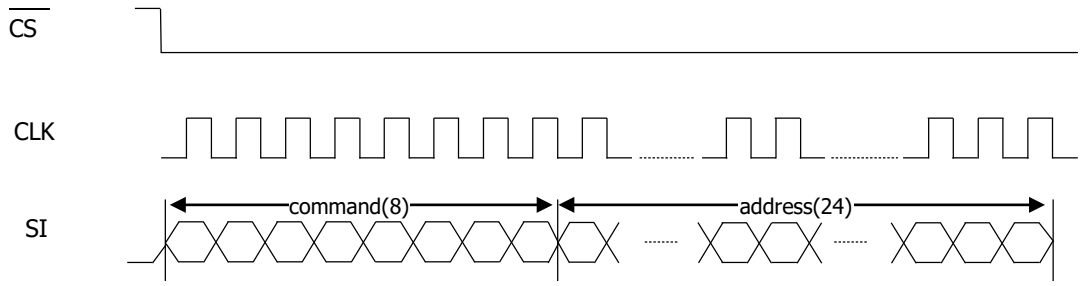
Figure 8 : Description of DDR Instruction Type



Instruction Structure

- Each instruction starts out with an 8-bit command. The command selects the type of operation.
  The instruction can be stand alone or followed by address to select a memory location or register.
  The address is always 24-bits wide.

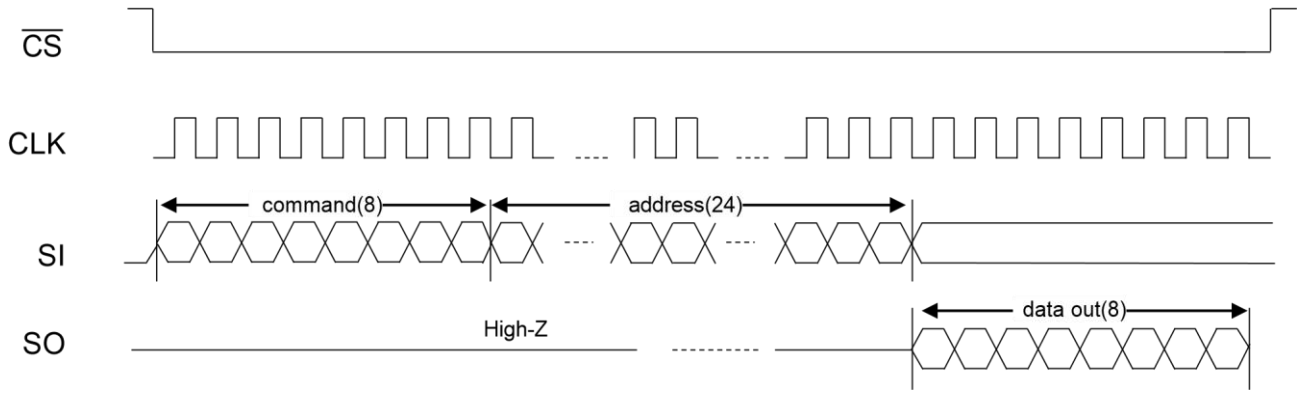
Figure 9 : Description of command followed by Address (SSIP mode)



Read Operation

- Read operation starts from pulling $\overline{CS}$ Low.
  8 bits Read command(03h) is transmitted to the device then
  24 bit address is following while the first 7 MSB bits of address are don't care.
  The device outputs the data at selected address to the SO pin. The read operation can be terminated by pulling $\overline{CS}$ high.

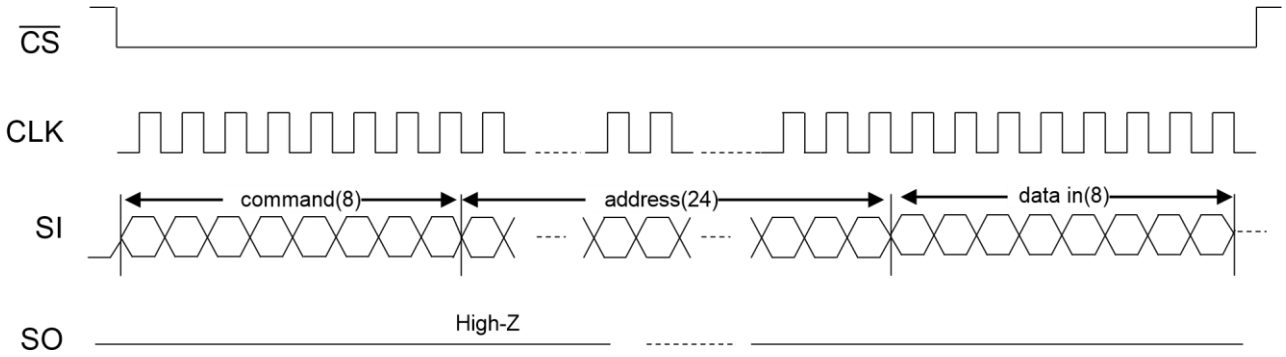
Figure 10 : Description of Read Operation (SSIP mode)



Write Operation

- Write operation starts from pulling $\overline{CS}$ Low. 8 bits Write command(02h) is transmitted to the device then 24 bit address is following while the first 7 MSB bits of address are don't care. The data on the SI pin is written to the device at selected address. The write operation can be terminated by pulling $\overline{CS}$ high.

Figure 11 : Description of Write Operation (SSPI mode)

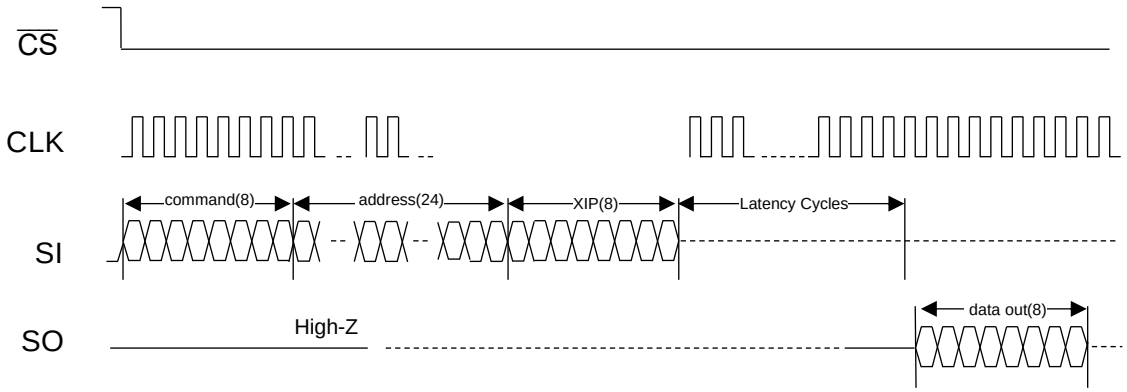


*** Notes :**
In normal operational mode, Write instructions must be preceded by the WREN command.
WREN command sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction.
WREN bit can also be reset by executing the WRDI command.
The device offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array or the augmented 512-byte area.
These modes are set in Configuration Register 4.

XIP (Execute In Place) Operation

- For read and write operation, the device offers XIP (execute in place) mode.
  XIP allows a series of read or write operation without loading individual read or write command for each instruction, which results in reduced random access time. XIP is enabled by entering byte AXh and disabled by entering any byte not equal to AXh. These respective bytes must be entered following the address bits.
  Read operation with XIP needs extra Read-Latency before data coming out from SO pin.
  The latencies are specified in Table 18 : Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP) .

Figure 12 : Description of Read Operation with XIP (SSIP mode)



Continuing Read/Write

- The entire memory array can be read from or written to using a single read or write instruction.
  After the starting address is entered, subsequent address are internally incremented as long as $\overline{CS}$ is Low and CLK continues toggling.

Figure 13 : Description of Continuing Read Operation (SSIP mode)

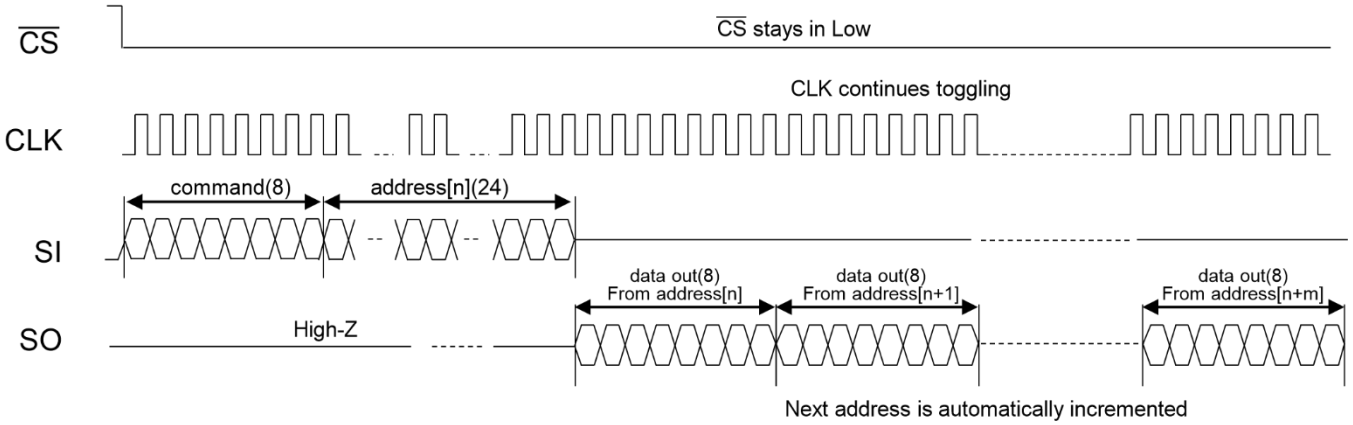
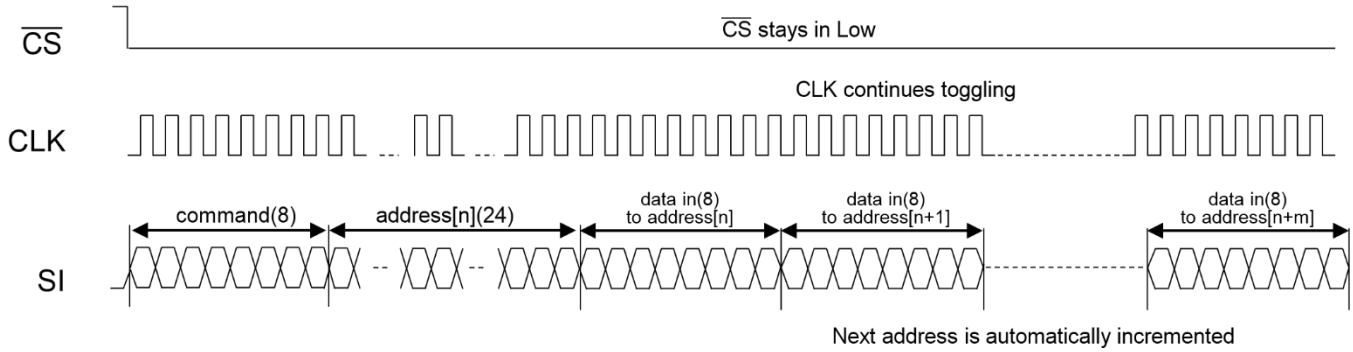


Figure 14 : Description of Continuing Write Operation (SSIP mode)

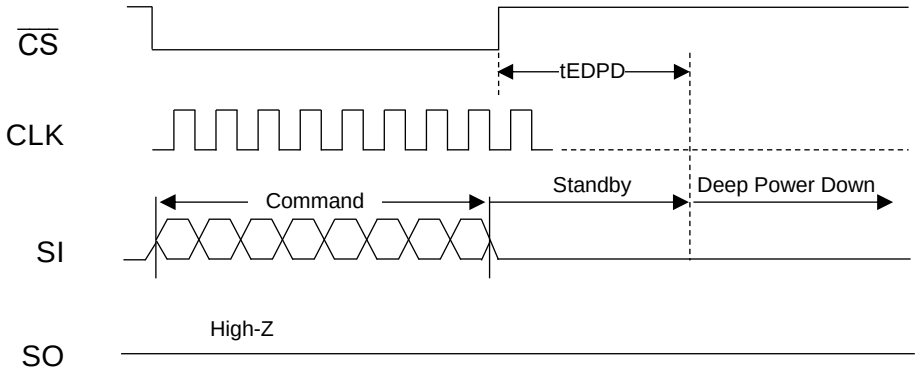


- For read operation, the device offers wrap mode. Wrap bursts are confined to address aligned 16/32/64/128/256/512/1K byte boundary.
  he read address can start anywhere within the wrap boundary.
  16/32/64/128/256/512/1K wrap configuration is set in Configuration Register 3.

Deep Power Down Modes

- The device provides Deep Power Down mode. This mode reduces current consumption from ISB to IDPD.
  To enter the deep power down mode, $\overline{CS}$ is driven low, following the enter Deep Power Down (DPDE) command, $\overline{CS}$ must be driven high after the eighth bit of the command code has been latched in or the DPDE command will not be executed.
  After $\overline{CS}$ is driven high, it requires a delay of t_{EDPD} before the supply current is reduced to IDPD and the Deep Power Down mode is entered. The command can be issued in SPI, DSPI or QSPI modes.

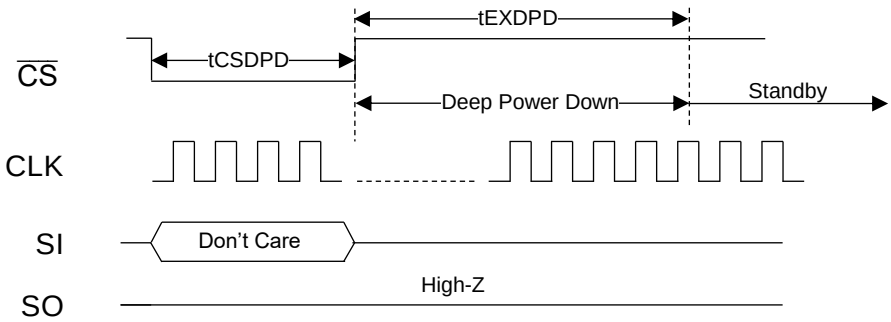
Figure 15 : Entering Deep Power Down Mode (SSIP mode)



- There are two ways to exit deep power down mode:

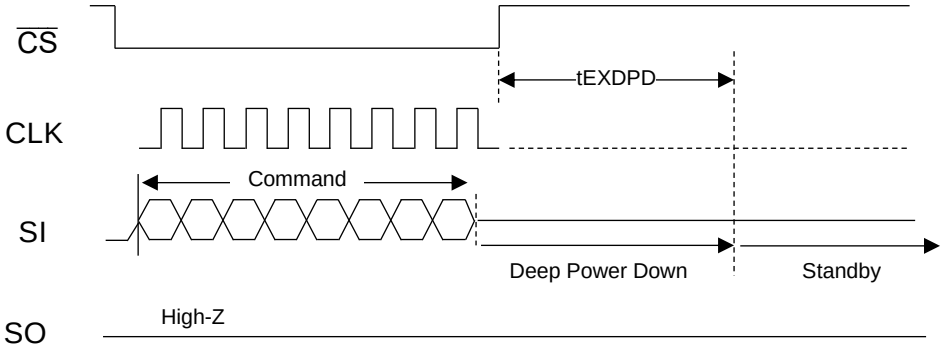
1. Toggling $\overline{CS}$ with a $\overline{CS}$ pulse width of t_{CSDPD} while CLK and I/Os are Don't Care. During waking up from deep power down, I/Os remain to be in high-Z.

Figure 16 : Exit Deep Power Down Mode by $\overline{CS}$



2. Driving $\overline{CS}$ low follows with the Exit Deep Power Down (EXDPD, ABh) command. $\overline{CS}$ must be driven high after the eight bit of the command code has been latched in or the EXDPD command will not executed.

Figure 17 : Exit Deep Power Down Mode by SPI Command

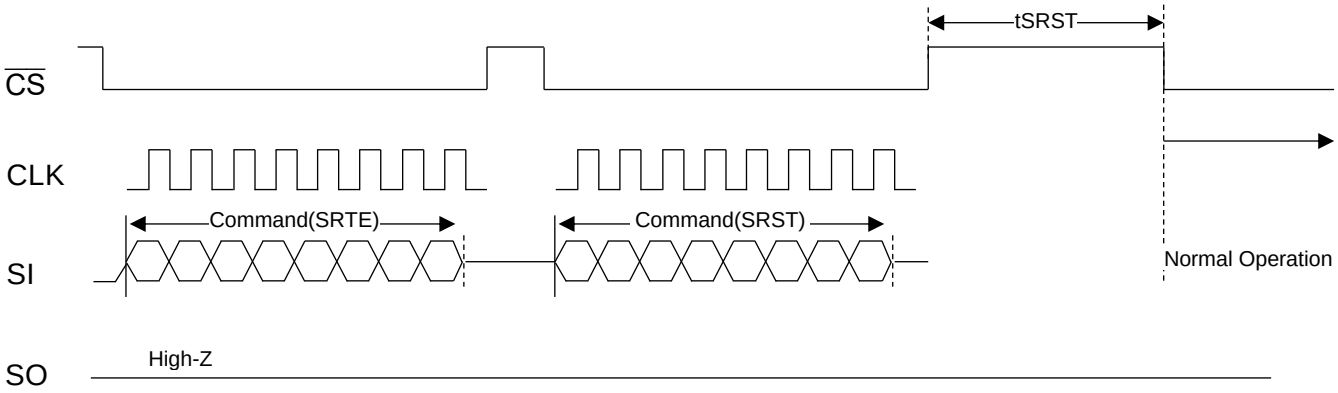


- It requires a delay of t_{EXDPD} before the device can fully exit the deep power down mode and enter standby mode.
- Status of all non-volatile bits in registers remains unchanged when the device enters or exits the deep power down mode.
- The command can be issued in SPI, DPI, and QPI mode.

Software Reset

Software Reset (SRST) requires Software Reset Enable (SRTE) implemented in advance.

Figure 18 : Software Reset Timing



JEDEC Reset

Figure 19 : JEDEC Reset Operation Timing

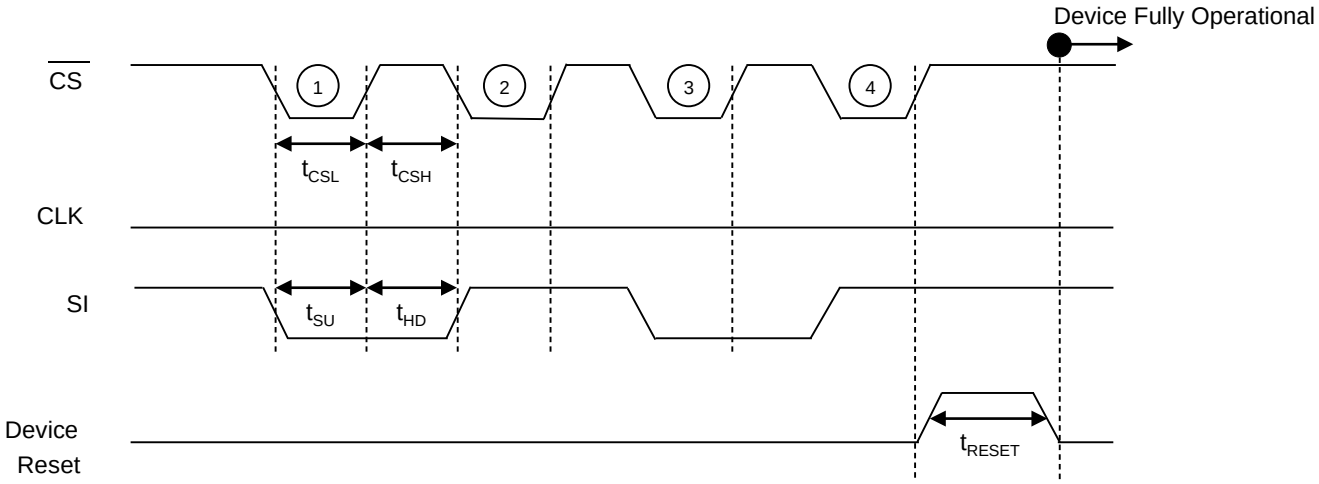


Table 27 : JEDEC Reset Operation & Timing : 1.8V Device

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Low Time	t_{CSL}	0.5	-	µs
$\overline{CS}$ High Time	t_{CSH}	0.5	-	µs
SI Setup Time (w.r.t $\overline{CS}$)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t $\overline{CS}$)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	2.0	ms

Electrical Specifications

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device.
This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 28 : Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage on Vcc Supply Relative to VSS : 1.8V Device	-0.5	2.35	V
Voltage on Any Pin relative to VSS : 1.8V Device	-0.5	2.35	V
Storage Temperature	-55	150	°C
Operating Ambient Temperature	-40	85	°C
ESD HBM (Human Body Model)	≥ |2000 V|		V
ESD CDM (Charged Device Model)	≥ |500 V|		V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles - Peak temperature ≤ 260°C - The time above 255°C ≤ 30 seconds - Reflow cycles ≤ 3 times		

Endurance, Retention and Magnetic Immunity

Table 29 : Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Units
Write Endurance	-25°C	10^{14}	-	cycles
Data Retention	85°C	20	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

Recommended Operating Conditions

Table 30 : Recommended Operating Conditions

Parameter / Condition		Min.	Typ.	Max.	Units
Operating Temperature	Industrial	-40	25	85	°C
Vcc Supply Voltage : 1.8V Device		1.71	1.8	1.98	V
Vss Supply Voltage		0.0	0.0	0.0	V

Pin Capacitance

Table 31 : Pin Capacitance

Parameter	Conditions	Typ.	Max.	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	-	6	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; $V_{I/O}$ = 0V	-	10	pF

Note : Capacitance is sampled and not 100% tested

AC Test Condition

Table 32 : AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	1ns/1V
Input and output measurement timing levels	Vcc/2
Output Load	CL = 30pF

DC Characteristics

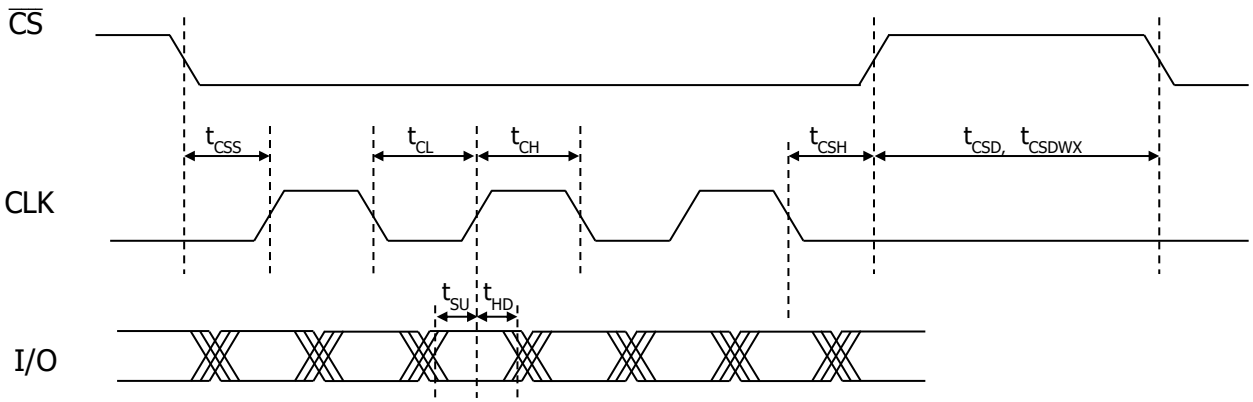
Table 33 : DC Characteristics : 1.8V Device

Parameter	Symbol	Test Conditions	1.71V~1.98V			Units
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to Vcc (max)	-2	-	2	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to Vcc (max)	-2	-	2	µA
Read Current (1-1-1)	I_{CCR4}	SDR=133MHz, DDR=67MHz $\overline{CS}$=0, CLK=0/Vcc, I_{OUT}=0mA	-	5	8	mA
Read Current (2-2-2)	I_{CCR5}		-	8	11	mA
Read Current (4-4-4)	I_{CCR6}		-	10	14	mA
Write Current (1-1-1)	I_{CCW4}	SDR=133MHz, DDR=67MHz $\overline{CS}$=0, CLK=0/Vcc, I/O=0/Vcc	-	11	13	mA
Write Current (2-2-2)	I_{CCW5}		-	15	19	mA
Write Current (4-4-4)	I_{CCW6}		-	25	30	mA
Standby Current	I_{SB}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	560	900	µA
Deep Power Down Current	I_{DPD}	CLK=0, $\overline{CS}$ = Vcc, I/O=0/Vcc	-	60	280	µA
Input High Voltage	V_{IH}	-	0.7xVcc	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.3xVcc	V
Output High Voltage Level	V_{OH}	I_{OH} = -1mA	1.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2mA	-	-	0.4	V

AC Timing Characteristics

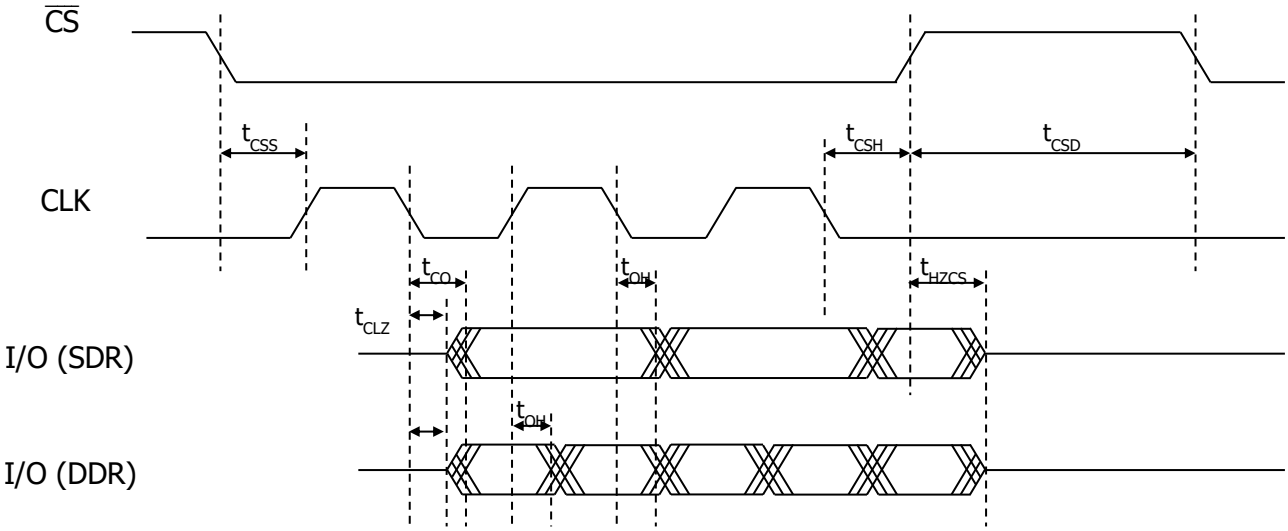
Synchronous Input Timing

Figure 20 : Synchronous Input Timing (SDR/DDR)



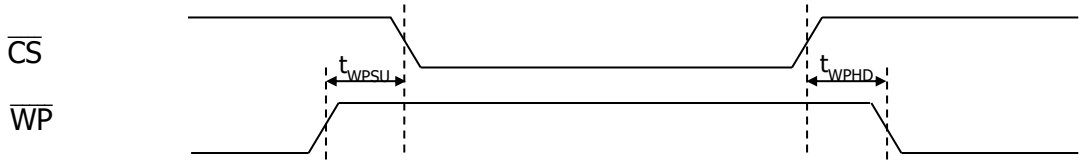
Synchrounous Data Output Timing

Figure 21 : Synchronous Data Output Timing (SDR/DDR)



WP Timing

Figure 22 : WP Operation Timing



$\overline{CS}$ High Time

Figure 23 : $\overline{CS}$ High Timing

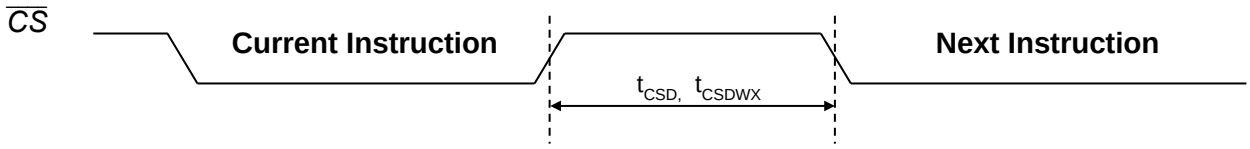


Table 34 : $\overline{CS}$ High Time after Write Instruction : SDR=133MHz/DDR=67MHz

Current Instruction : Main Array Write	Next Instruction : Main Array Read or Write	Symbol	Min.	Units
(1-1-1), (1-x-2)	(1-1-x)	t_{CSDW1}	20	ns
(1-1-1), (1-x-2)	(1-2-2)	t_{CSDW2}	80	ns
(1-x-4)	(1-1-x)	t_{CSDW3}	80	ns
(1-1-1), (1-x-2)	(1-4-4)	t_{CSDW4}	150	ns
(1-x-4)	(1-2-2), (1-4-4)	t_{CSDW5}	240	ns
(2-2-2)	(2-2-2)	t_{CSDW6}	150	ns
(4-4-4)	(4-4-4)	t_{CSDW7}	290	ns

Table 35 : $\overline{CS}$ High Time after Register/Augmented 512-Byte Area Write Instruction

Current Instruction	Next Instruction	Symbol	Min.	Units
Main Array Write Instruction	Register Read/Write Augmented 512-Byte Read/Write	t_{CSDW12}	500	ns
Register Write Augmented 512-Byte Write	Any Instructions	t_{CSDW13}	1000	ns

Note 1: RDSR(05h) instruction is applicable during t_{CSDWX}.

AC Timing Parameters

Table 36 : AC Timing Parameter

Parameter	Symbol	Min.	Max.	Units
Clock Frequency – SDR	f_{CLK}	1	133	MHz
Clock Frequency – DDR	f_{CLK}	1	67	MHz
Clock Low Time	t_{CL}	0.45 * 1/ fCLK	-	ns
Clock High Time	t_{CH}	0.45 * 1/ fCLK	-	ns
$\overline{CS}$ Setup Time	t_{CSS}	5	-	ns
$\overline{CS}$ Hold Time	t_{CSH}	4	-	ns
$\overline{CS}$ High Time after Any Instruction (except Write)	t_{CSD}	20	-	ns
$\overline{CS}$ High Time after Write Instruction	t_{CSDWx}	Refer to Table 34, 35		ns
Data Setup Time	t_{SU}	2	-	ns
Data Hold Time	t_{HD}	2	-	ns
CLK Low to Output Valid	t_{CO}	-	7.0	ns
CLK to Output Hold Time	t_{OH}	2.0	-	ns
CLK Low to Output Low Z (Read)	t_{CLZ}	2.0	-	ns
$\overline{CS}$ High to Output High Z	t_{HZCS}	-	6.0	ns
$\overline{WP}$ Setup Time	t_{WPSU}	20	-	ns
$\overline{WP}$ Hold Time	t_{WPHD}	20	-	ns
$\overline{CS}$ High to Power-down mode	t_{EDPD}	-	1	us
$\overline{CS}$ High to Power-down mode exit	t_{EXDPD}	-	25	us
$\overline{CS}$ Low time to exit Power-down mode	t_{CSDPD}	50	-	ns
Software Reset Time (1.8V Device)	t_{SRST}	-	2.0	ms

Thermal Resistance

Table 37 : Thermal Resistance

Parameter	Description	8-pad WSON	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	30.6	93.9	°C/W
θ_{JC}	Thermal resistance (junction to case)	19.0	31.9	

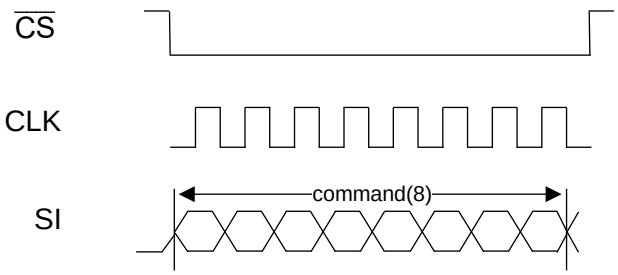
Notes:
1: These parameters are guaranteed by characterization; not tested in production.

Timing Description of Instruction Sets

Single SPI – SDR (Command-Address-Data)

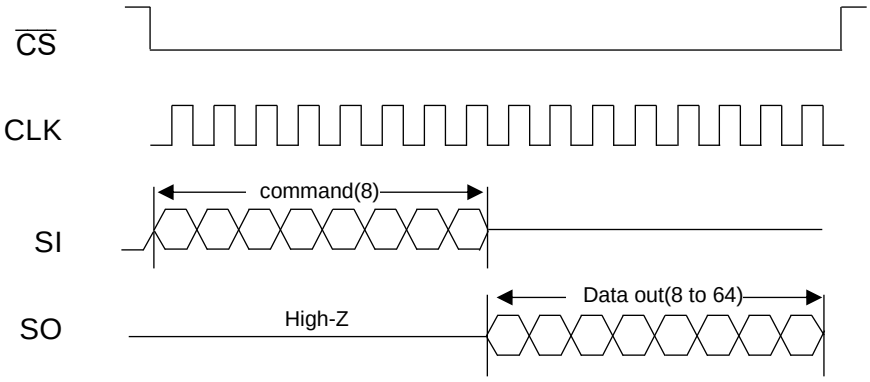
- Instruction 1-0-0 ; NOOP, WREN, WRDI, DPIE, QPIE, DPDE, DPDX, SRTE, SRST

Figure 24 : Timing Description of 1-0-0 Instruction Type



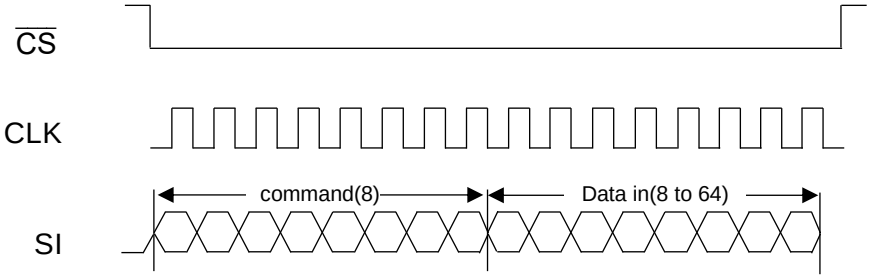
- Instruction 1-0-1 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

Figure 25 : Timing Description of 1-0-1 Instruction Type (Read)



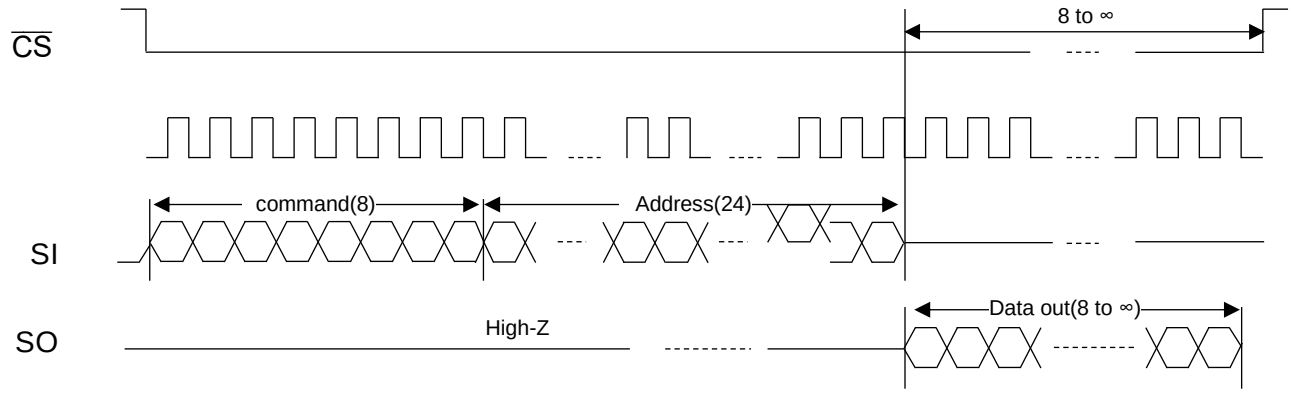
- Instruction 1-0-1 ; WRSR, WRCX, WRSN, WRAP

Figure 26 : Timing Description of 1-0-1 Instruction Type (Write)



- Instruction 1-1-1 ; READ(03h)

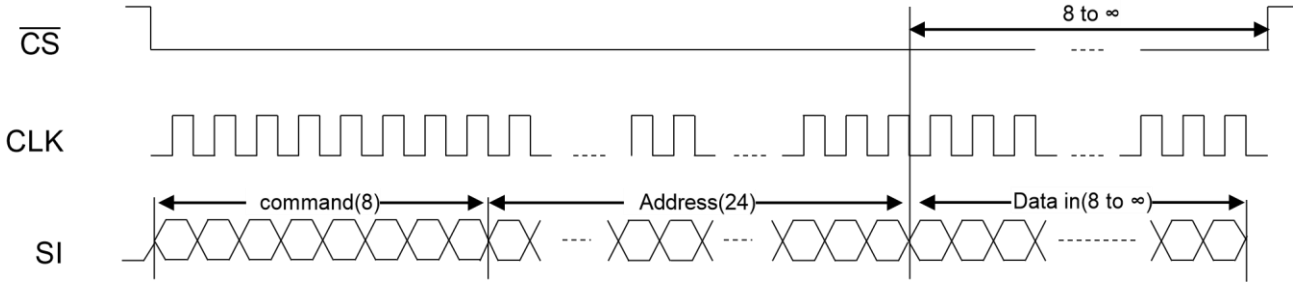
Figure 27 : Timing Description of 1-1-1 Instruction Type (Read without XIP)



Notes:
As long as $\overline{CS}$ stays in low and CLK keeps toggling, next target address is incremented automatically and the device keeps outputting data from memory array.

- Instruction 1-1-1 ; WRTE(02h)

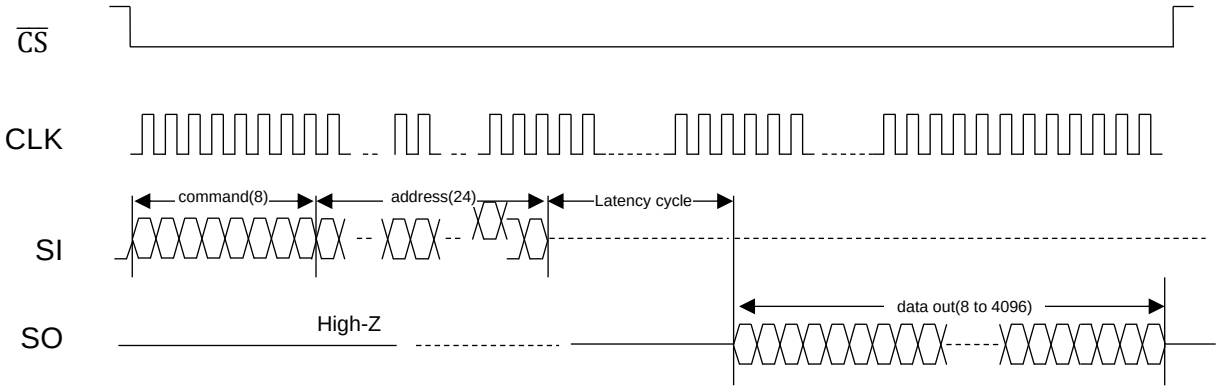
Figure 28 : Timing Description of 1-1-1 Instruction Type (Write)



Notes:
As long as $\overline{CS}$ stays in low and CLK keeps toggling, next target address is incremented automatically and the device keeps writing data to memory array.

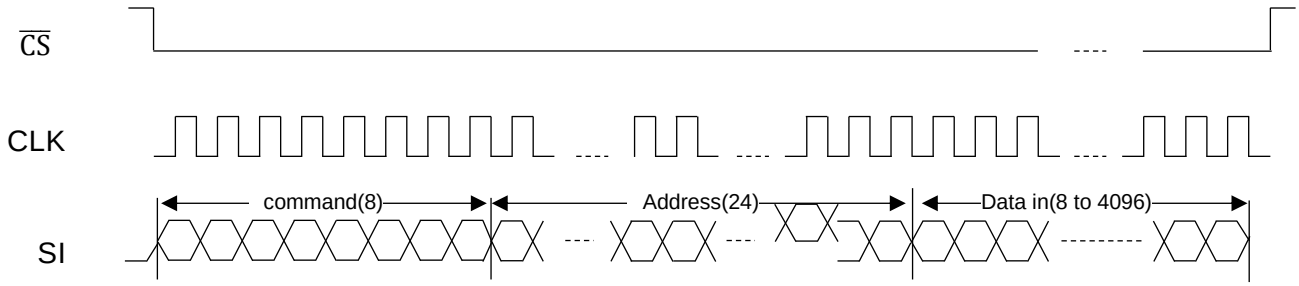
- Instruction 1-1-1 ; RDAS

Figure 29 : Timing Description of 1-1-1 Augmented 512-byte Area (Read)



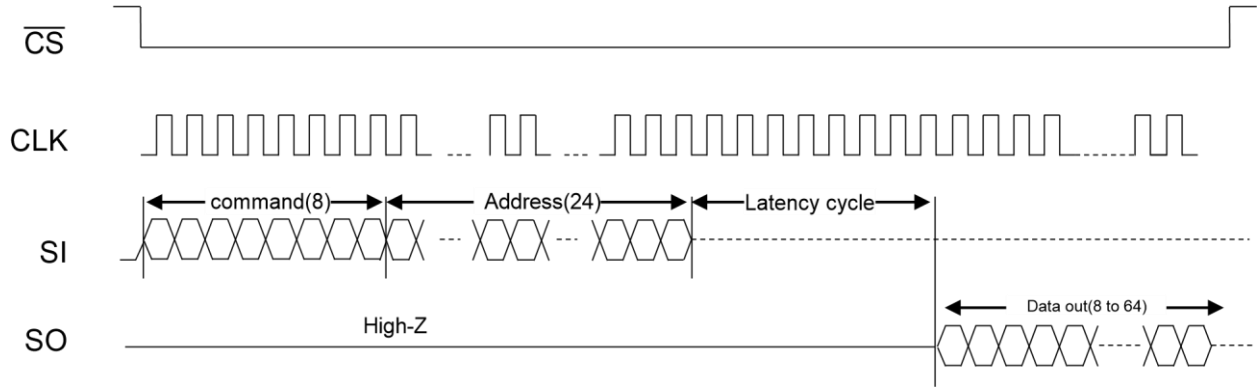
- Instruction 1-1-1 ; WRAS

Figure 30 : Timing Description of 1-1-1 Augmented 512-byte Area (Write)



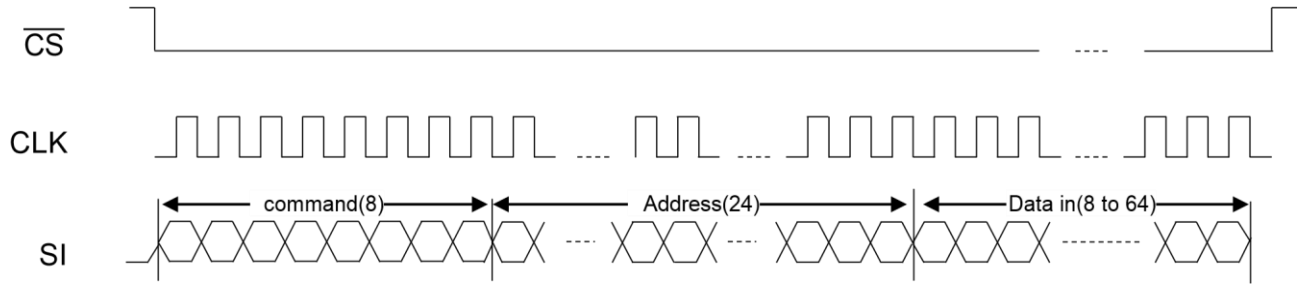
- Instruction 1-1-1 ; RDAR

Figure 31 : Timing Description of 1-1-1 Any Register Instruction Type (Read)



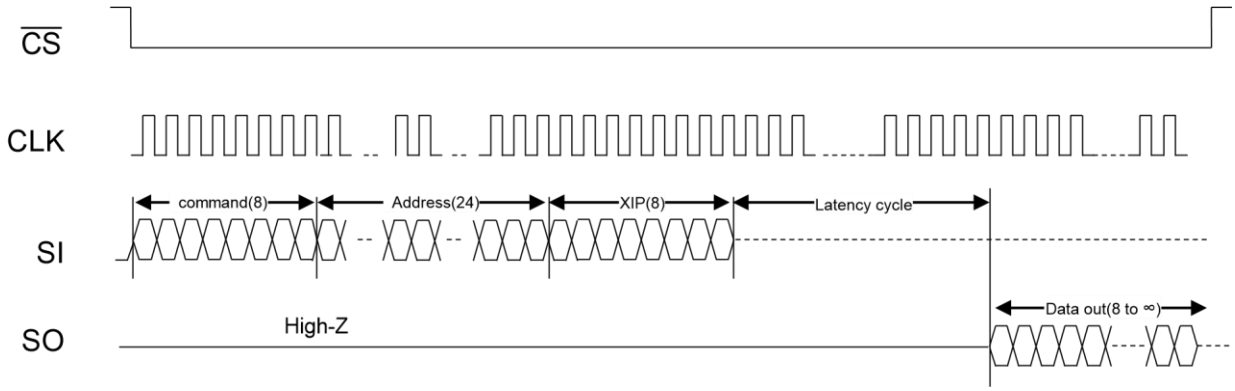
- Instruction 1-1-1 ; WRAR

Figure 32 : Timing Description of 1-1-1 Any Register Instruction Type (Write)



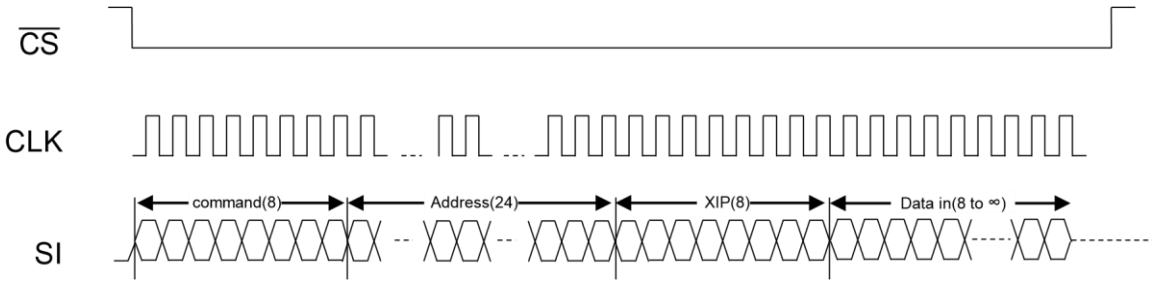
- Instruction 1-1-1 ; RDFT

Figure 33 : Timing Description of 1-1-1 Instruction Type (Read with XIP)



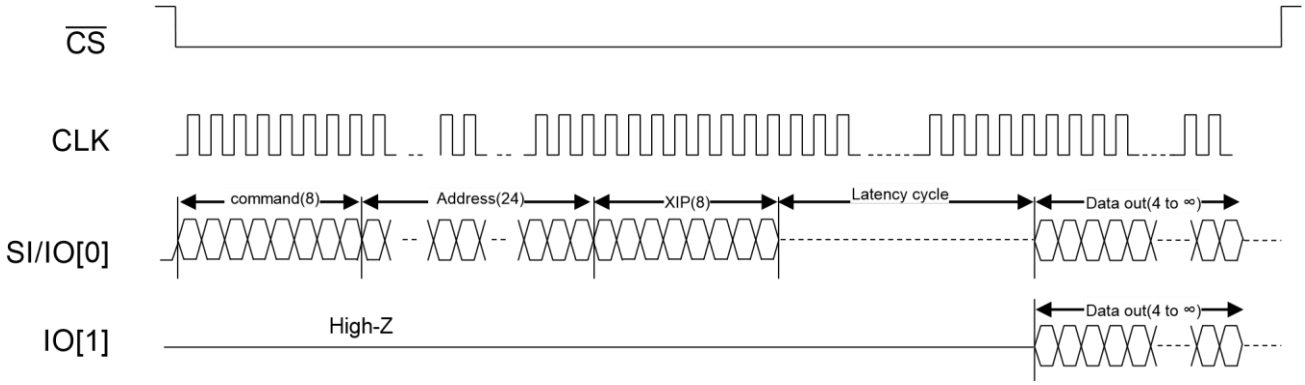
- Instruction 1-1-1 ; WRFT

Figure 34 : Timing Description of 1-1-1 Instruction Type (Write with XIP)



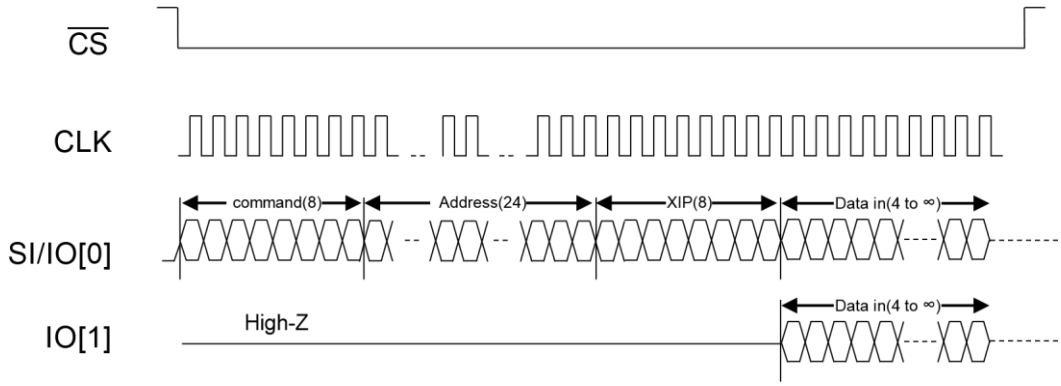
- Instruction 1-1-2 ; RDDO

Figure 35 : Timing Description of 1-1-2 Instruction Type (Read with XIP)



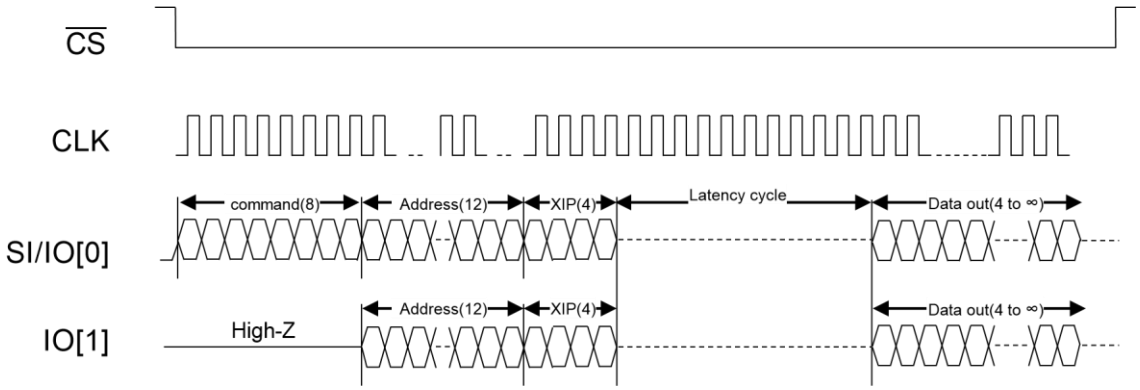
- Instruction 1-1-2 ; WDUI

Figure 36 : Timing Description of 1-1-2 Instruction Type (Write with XIP)



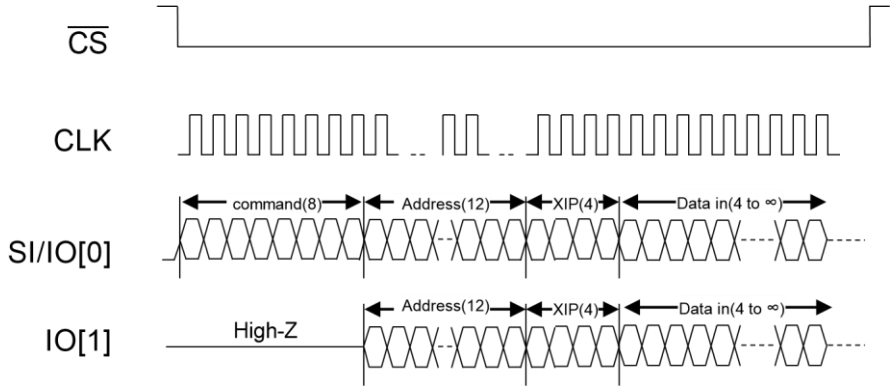
- Instruction 1-2-2 ; RDDI

Figure 37 : Timing Description of 1-2-2 Instruction Type (Read with XIP)



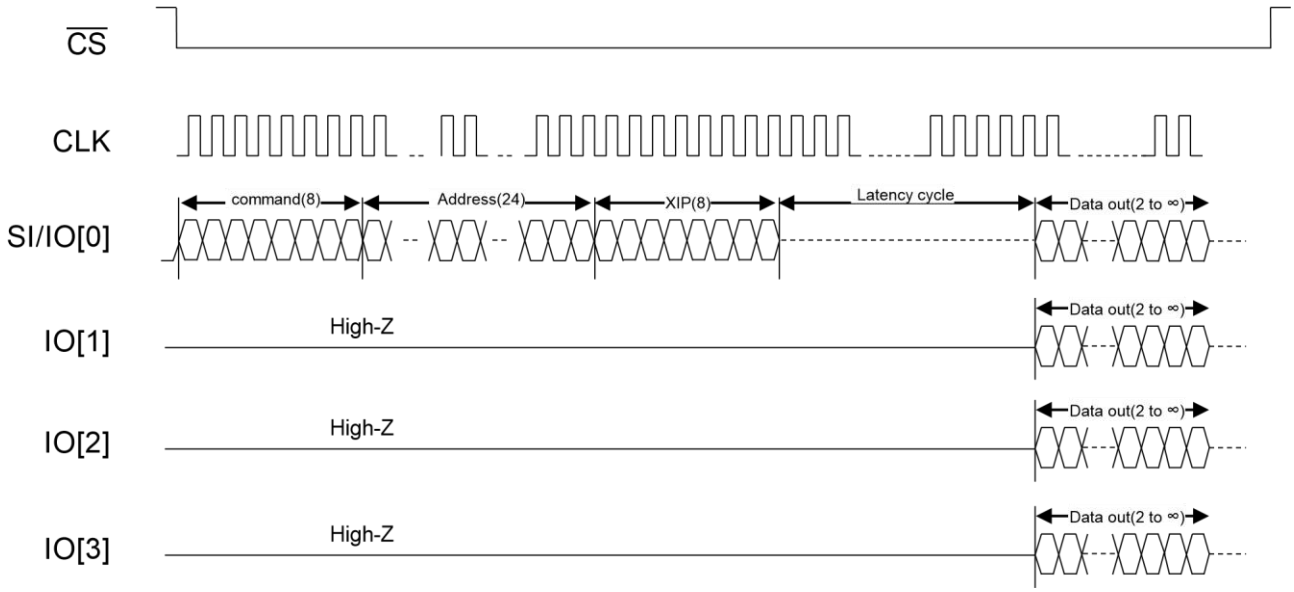
- Instruction 1-2-2 ; WDIO

Figure 38 : Timing Description of 1-2-2 Instruction Type (Write with XIP)



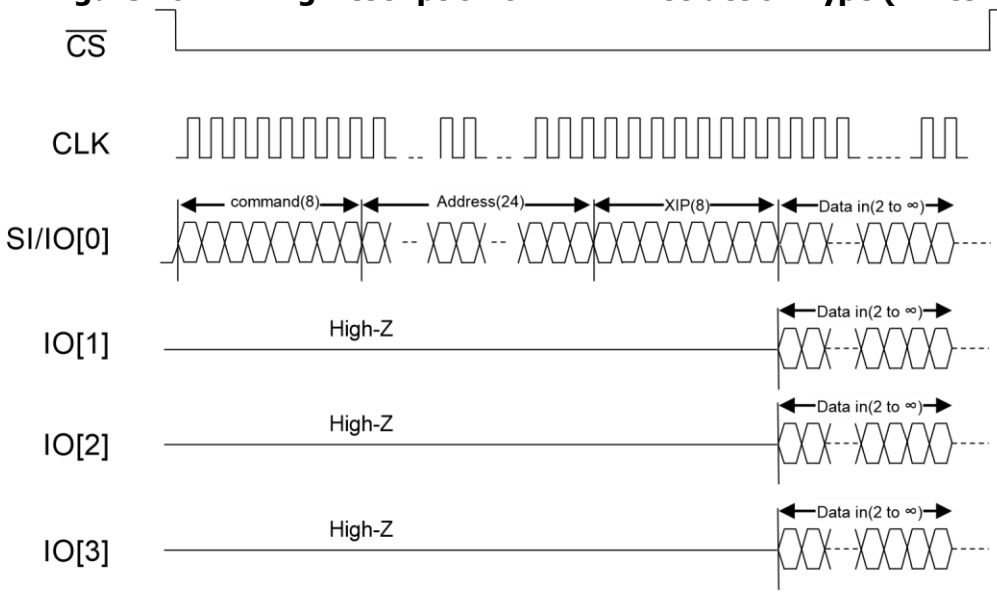
- Instruction 1-1-4 ; RDQO

Figure 39 : Timing Description of 1-1-4 Instruction Type (Read with XIP)



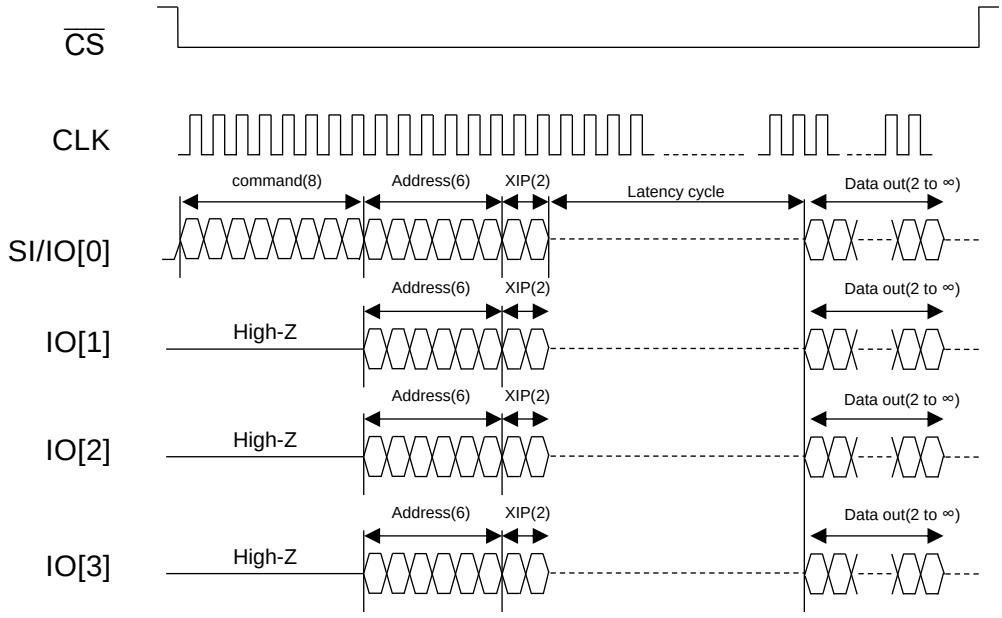
- Instruction 1-1-4 ; WQDI

Figure 40 : Timing Description of 1-1-4 Instruction Type (Write with XIP)



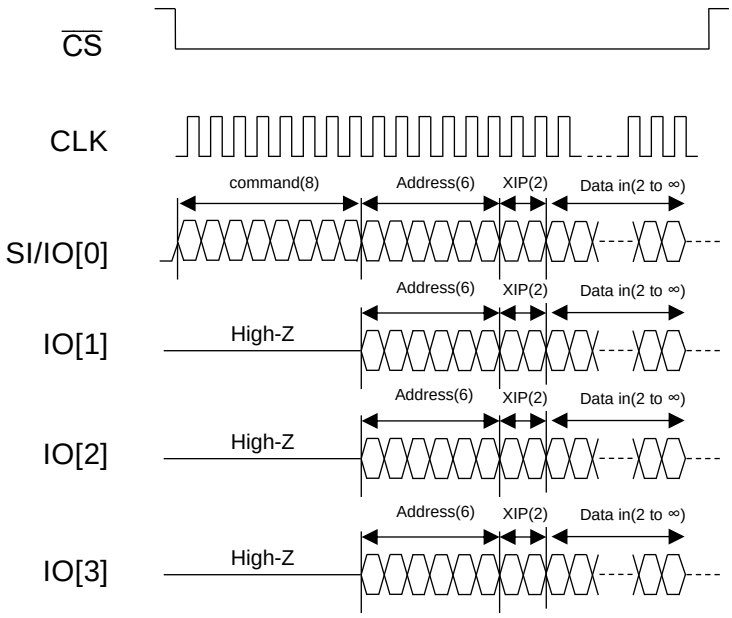
- **Instruction 1-4-4 ; RDQI**

Figure 41 : Timing Description of 1-4-4 Instruction Type (Read with XIP)



- **Instruction 1-4-4 ; WQIO**

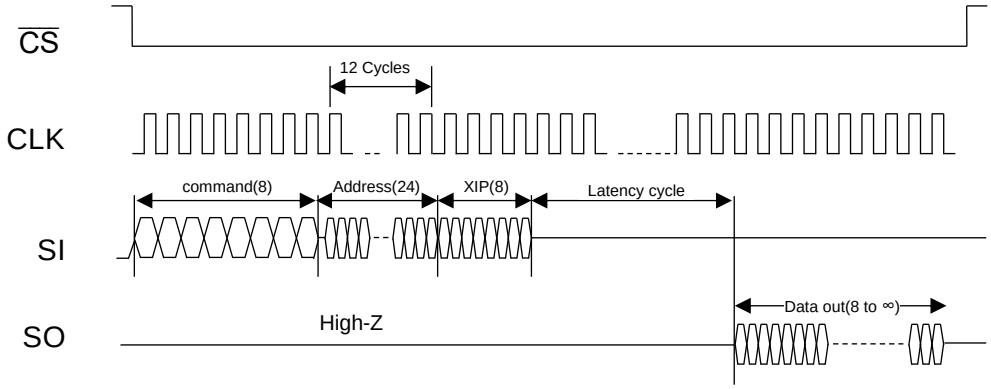
Figure 42 : Timing Description of 1-4-4 Instruction Type (Write with XIP)



Single SPI - DDR (Command-Address-Data)

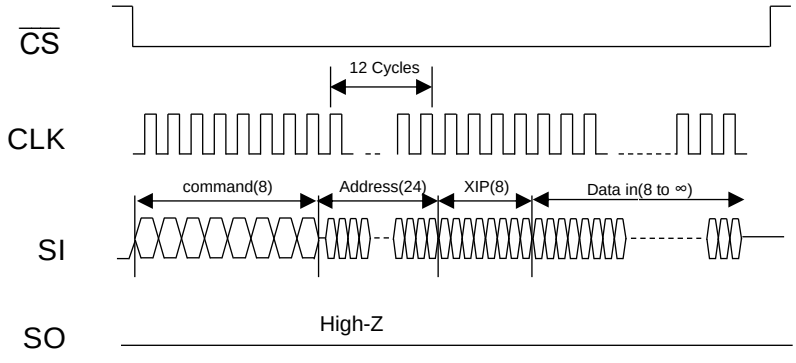
- Instruction 1-1-1 ; DRFR

Figure 43 : Timing Description of 1-1-1 DDR Instruction Type (Read with XIP)



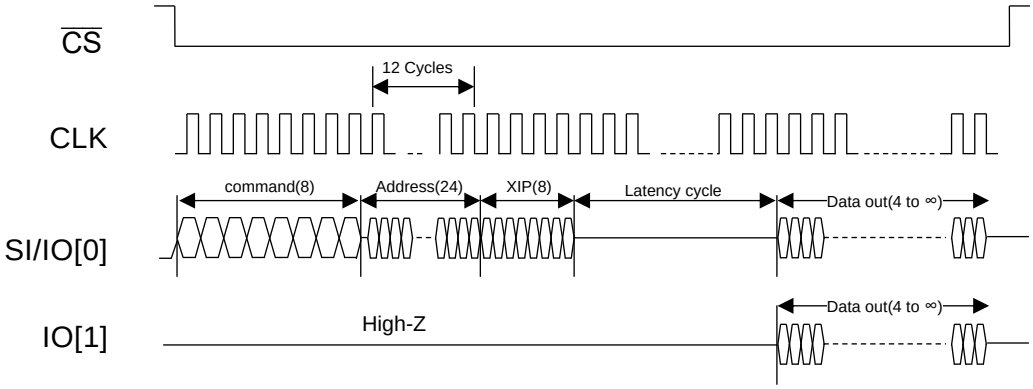
- Instruction 1-1-1 ; DRFW

Figure 44 : Timing Description of 1-1-1 DDR Instruction Type (Write with XIP)



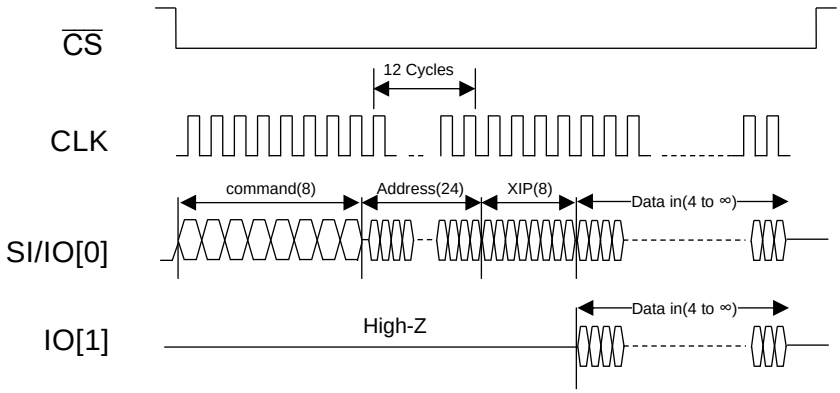
- Instruction 1-1-2 ; DRDO

Figure 45 : Timing Description of 1-1-2 DDR Instruction Type (Read with XIP)



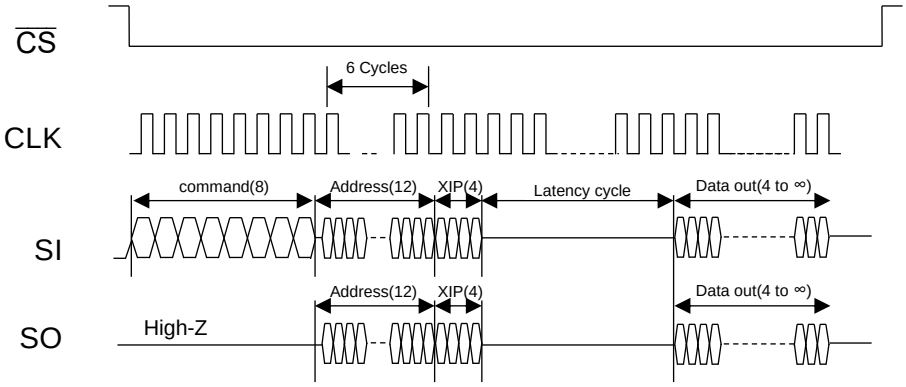
- Instruction 1-1-2 ; DWUI

Figure 46 : Timing Description of 1-1-2 DDR Instruction Type (Write with XIP)



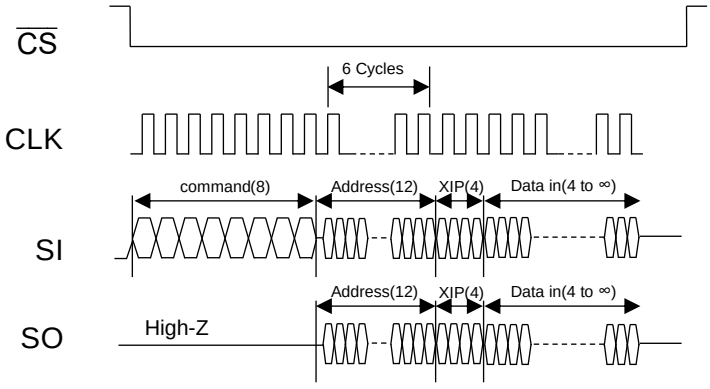
- Instruction 1-2-2 ; DRDI

Figure 47 : Timing Description of 1-2-2 DDR Instruction Type (Read with XIP)



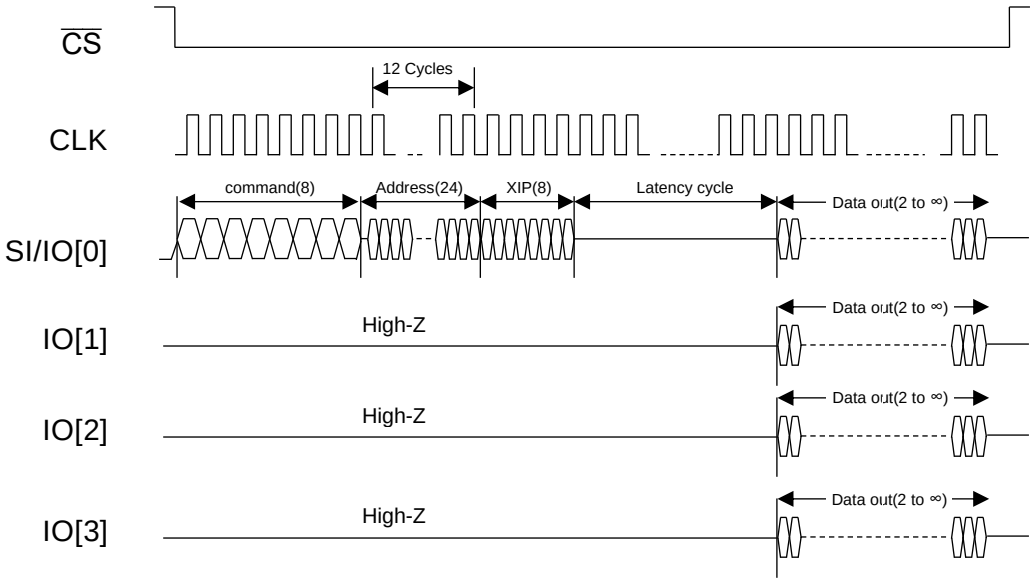
- Instruction 1-2-2 ; DWIO

Figure 48 : Timing Description of 1-2-2 DDR Instruction Type (Write with XIP)



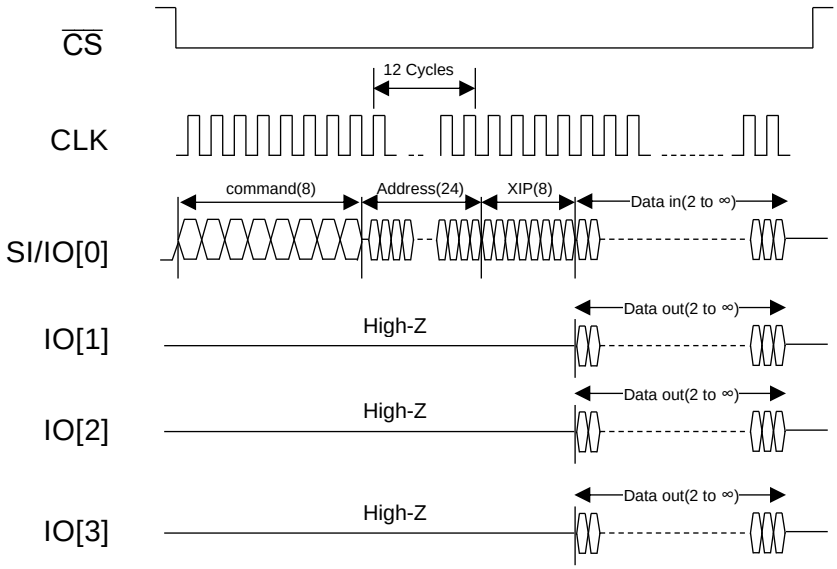
- Instruction 1-1-4 ; DRQO

Figure 49 : Timing Description of 1-1-4 DDR Instruction Type (Read with XIP)



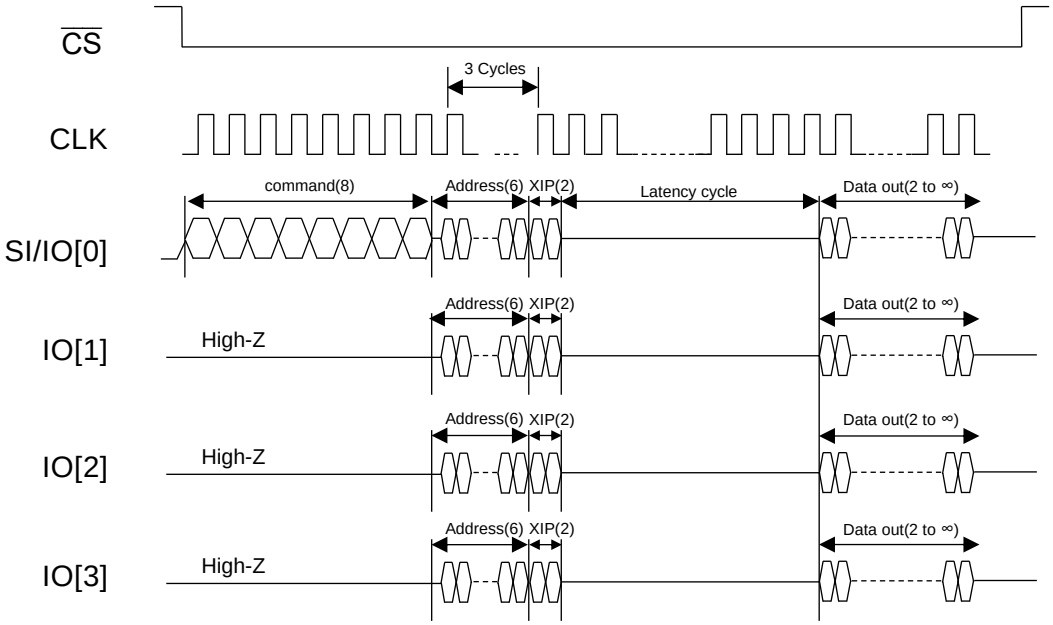
- Instruction 1-1-4 ; DWQI

Figure 50 : Timing Description of 1-1-4 DDR Instruction Type (Write with XIP)



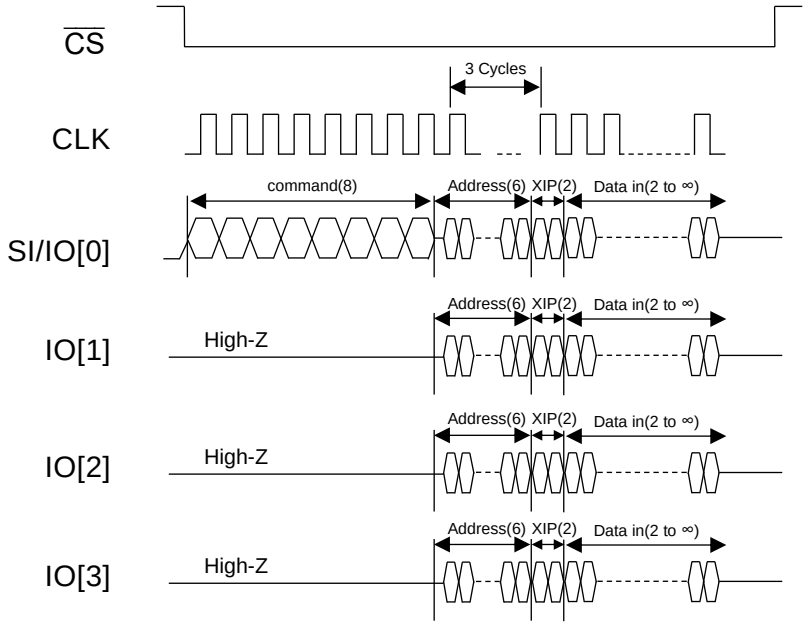
- Instruction 1-4-4 ; DRQI

Figure 51 : Timing Description of 1-4-4 DDR Instruction Type (Read with XIP)



- Instruction 1-4-4 ; DWQO

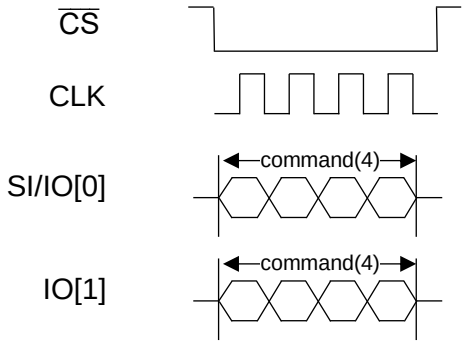
Figure 52 : Timing Description of 1-4-4 DDR Instruction Type (Write with XIP)



Dual SPI – SDR (Command-Address-Data)

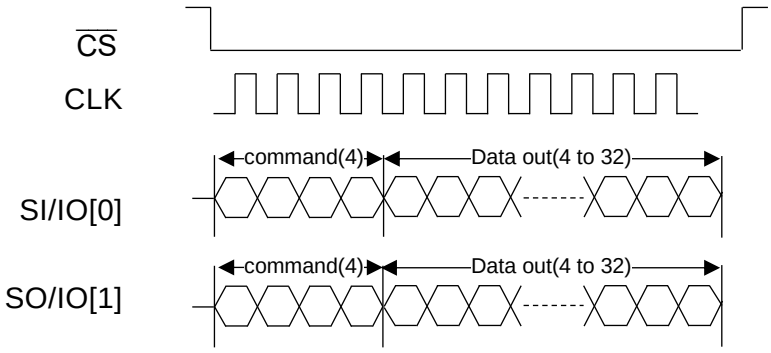
- Instruction 2-0-0 ; NOOP, WREN, WRDI, QPIE, SPIE, DPDE, DPDX, SRTE, SRST

Figure 53 : Timing Description of 2-0-0 Instruction Type



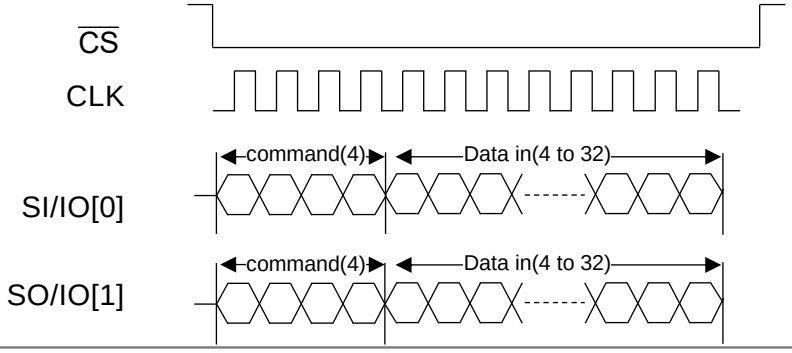
- Instruction 2-0-2 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

Figure 54 : Timing Description of 2-0-2 Instruction Type (Read)



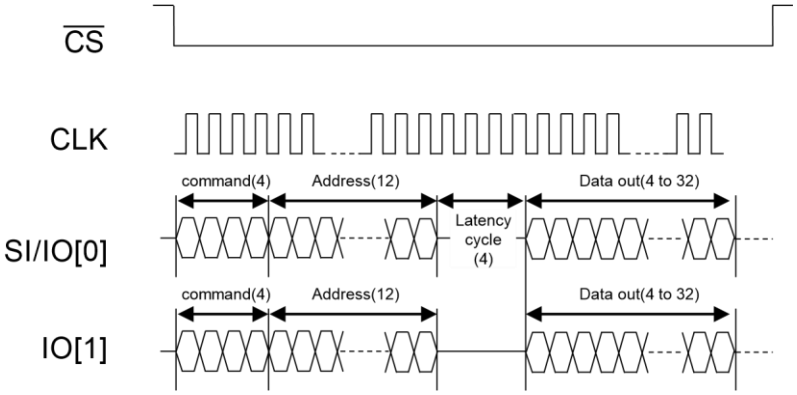
- Instruction 2-0-2 ; WRSR, WRCX, WRSN, WRAP

Figure 55 : Timing Description of 2-0-2 Instruction Type (Write)



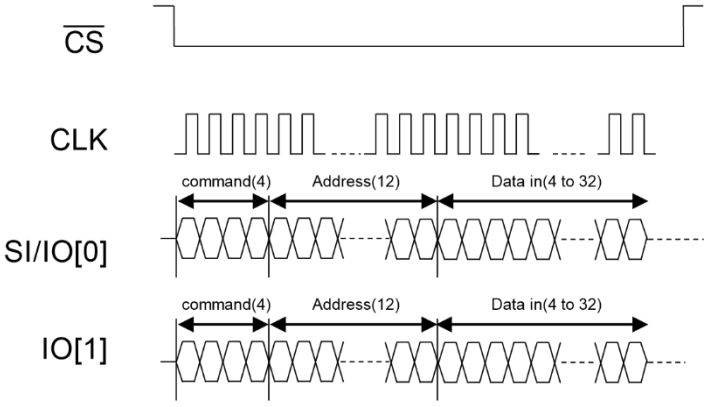
- Instruction 2-2-2 ; RDAR

Figure 56 : Timing Description of 2-2-2 Any Register Instruction Type (Read)



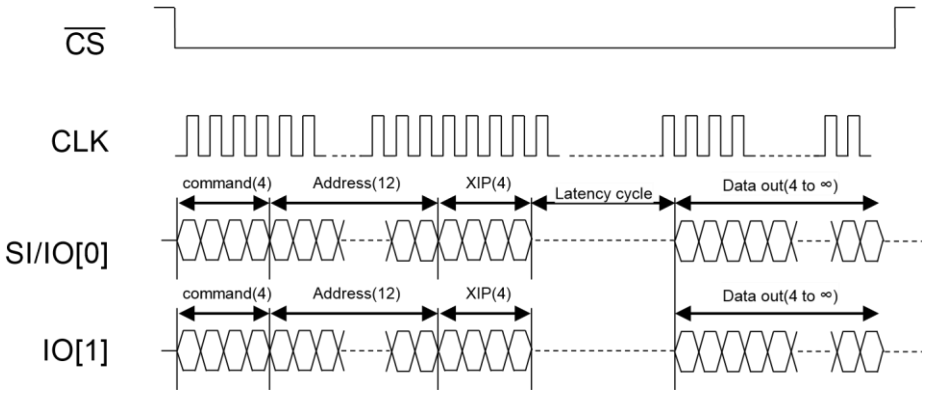
- Instruction 2-2-2 ; WRAR

Figure 57 : Timing Description of 2-2-2 Any Register Instruction Type (Write)



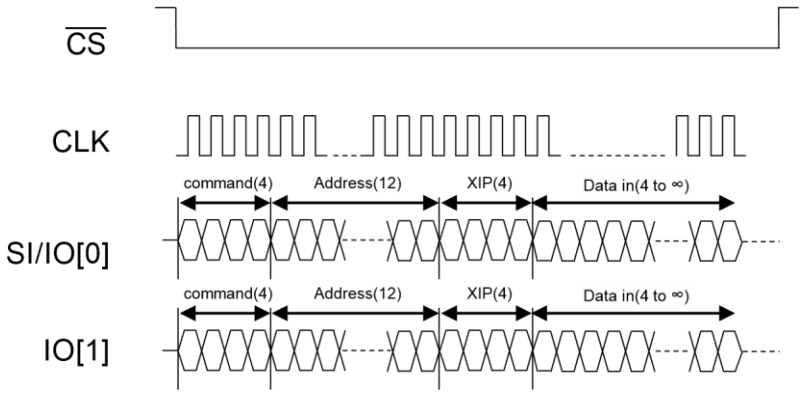
- Instruction 2-2-2 ; RDFT

Figure 58 : Timing Description of 2-2-2 Instruction Type (Read with XIP)



- Instruction 2-2-2 ; WRFT

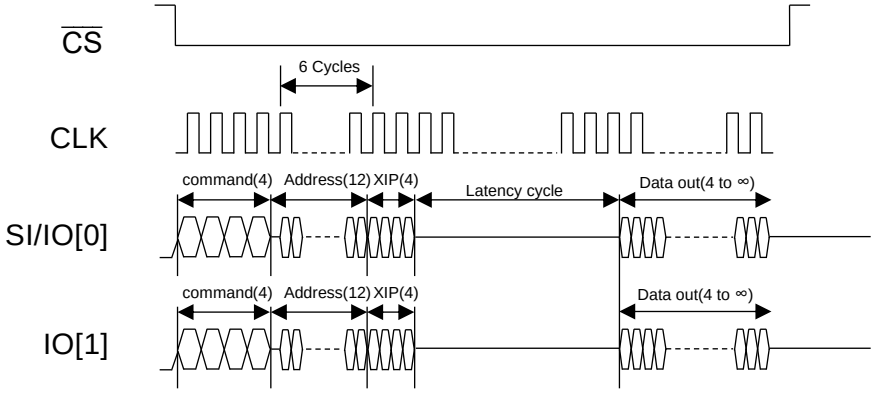
Figure 59 : Timing Description of 2-2-2 Instruction Type (Write with XIP)



Dual SPI - DDR (Command-Address-Data)

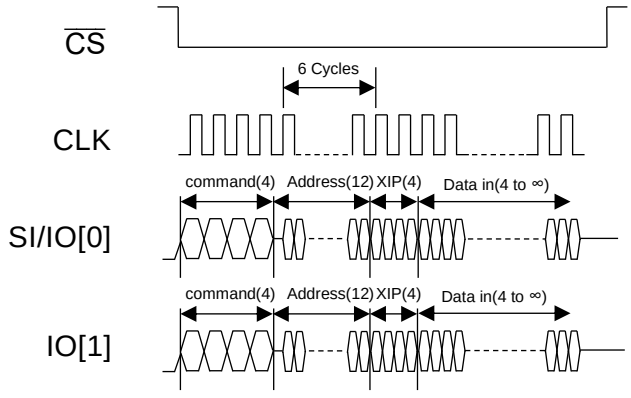
- Instruction 2-2-2 ; DRFR

Figure 60 : Timing Description of 2-2-2 DDR Instruction Type (Read with XIP)



- Instruction 2-2-2 ; DRFW

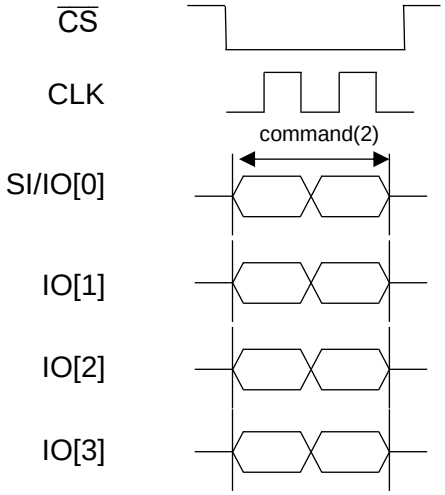
Figure 61 : Timing Description of 2-2-2 DDR Instruction Type (Write with XIP)



Quad SPI – SDR (Command-Address-Data)

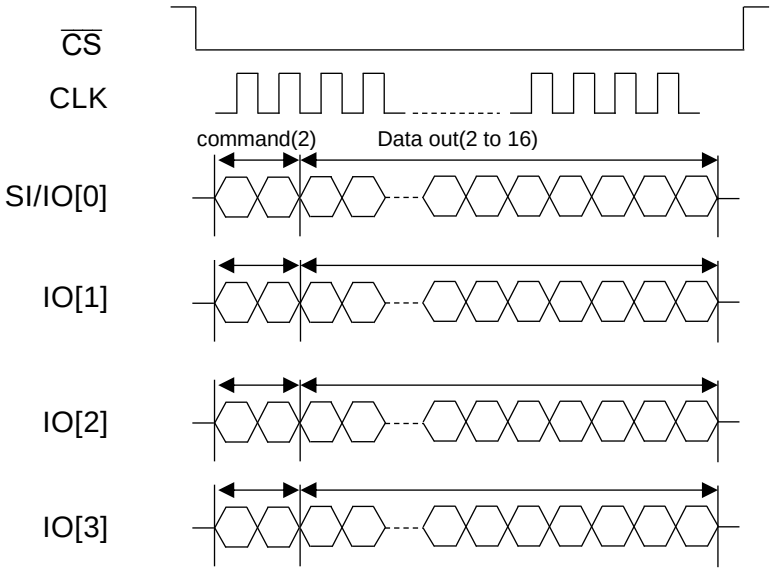
- Instruction 4-0-0 ; NOOP, WREN, WRDI, DPIE, SPIE, DPDE, DPDX, SRTE, SRST

Figure 62 : Timing Description of 4-0-0 Instruction Type



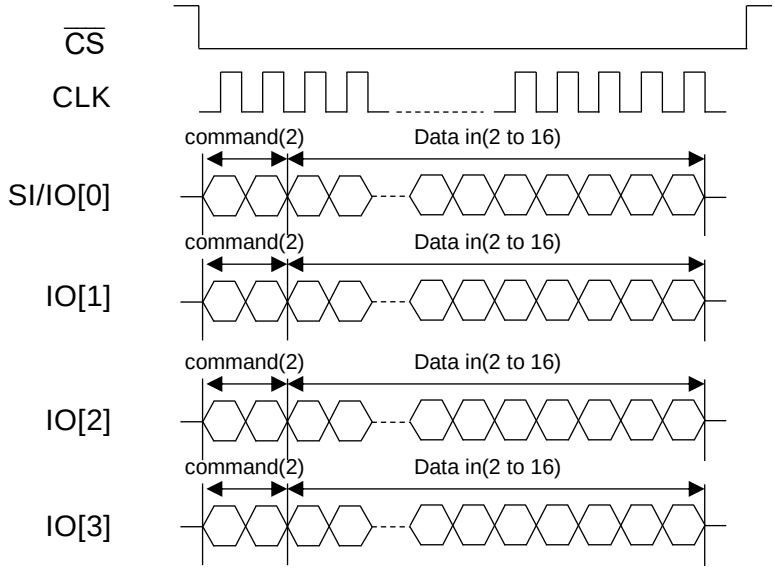
- Instruction 4-0-4 ; RDSR, RDC1, RDC2, RDC3, RDC4, RDCX, RDID, RUID, RDSN, RDAP

Figure 63 : Timing Description of 4-0-4 Instruction Type (Read)



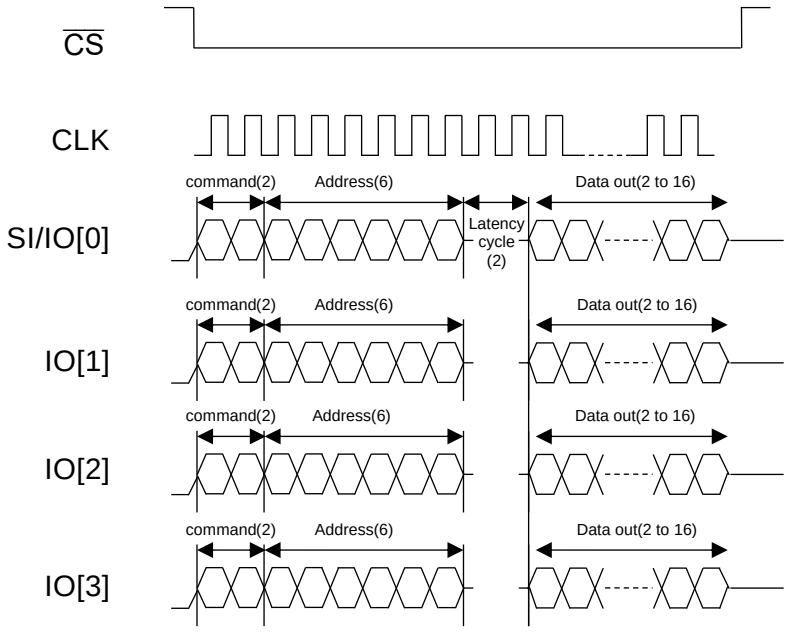
- Instruction 4-0-4 ; WRSR, WRCX, WRSN, WRAP

Figure 64 : Timing Description of 4-0-4 Instruction Type (Write)



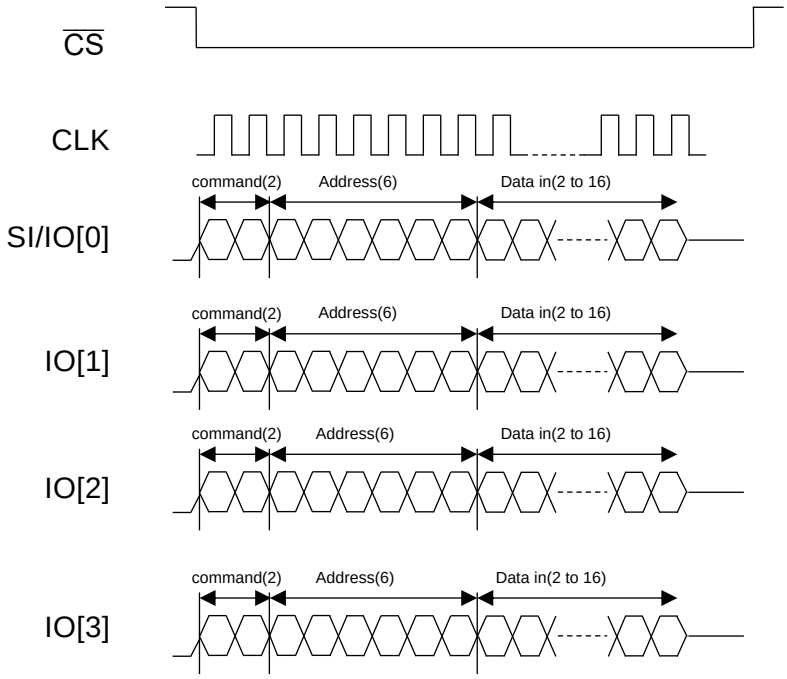
- Instruction 4-4-4 ; RDAR

Figure 65 : Timing Description of 4-4-4 Any Register Instruction Type (Read)



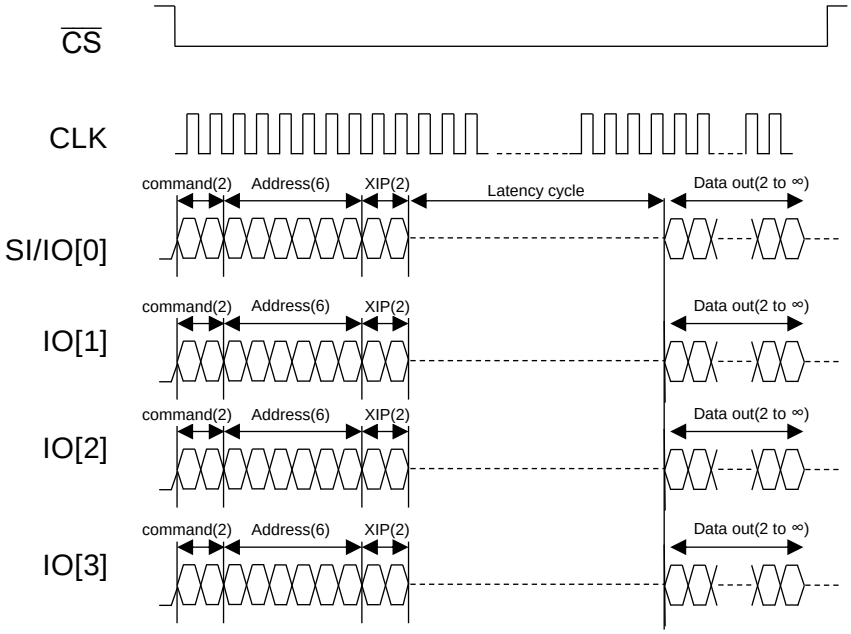
- Instruction 4-4-4 ; WRAR

Figure 66 : Timing Description of 4-4-4 Any Register Instruction Type (Write)



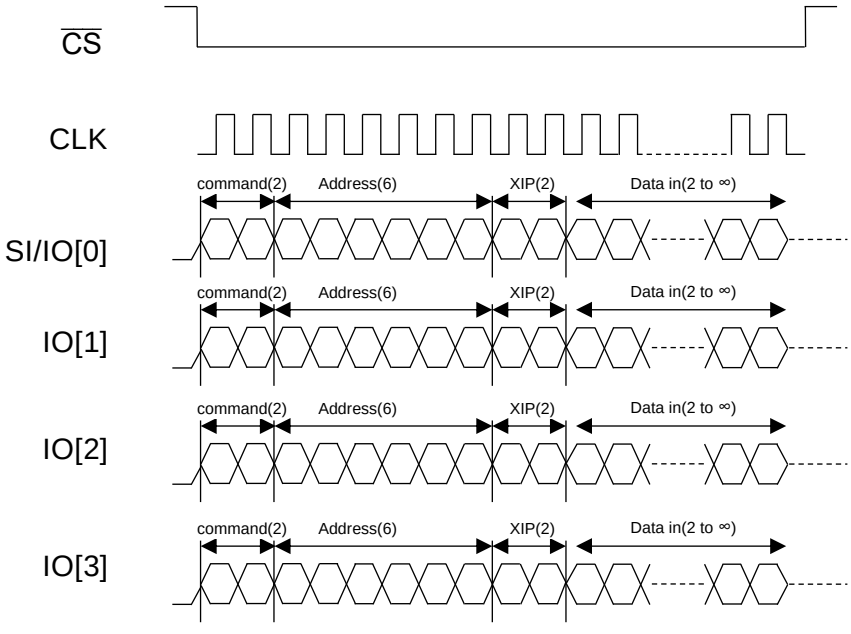
- Instruction 4-4-4 ; RDFT

Figure 67 : Timing Description of 4-4-4 Instruction Type (Read with XIP)



- Instruction 4-4-4 ; WRFT

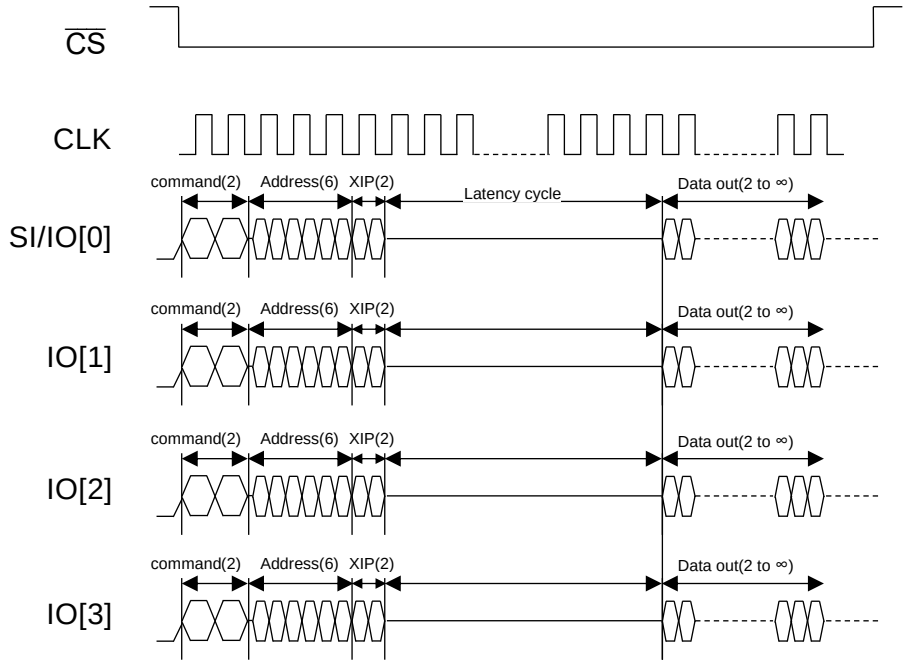
Figure 68 : Timing Description of 4-4-4 Instruction Type (Write with XIP)



Quad SPI - DDR (Command-Address-Data)

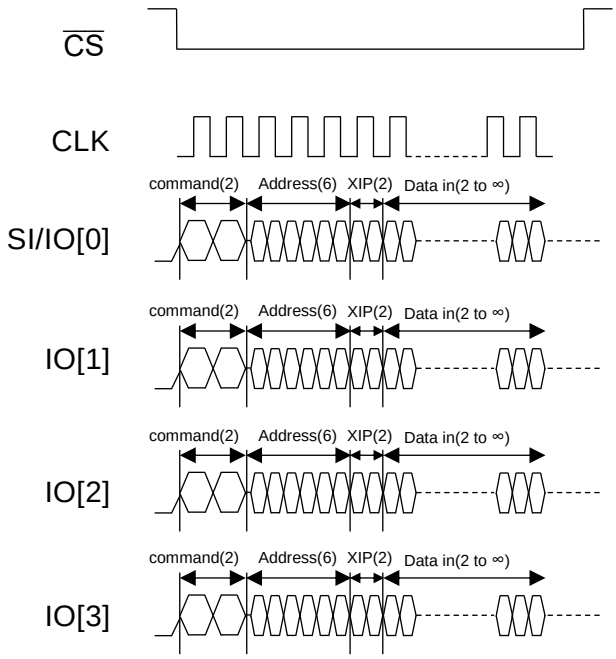
- Instruction 4-4-4 ; DRFR

Figure 69 : Timing Description of 4-4-4 DDR Instruction Type (Read with XIP)

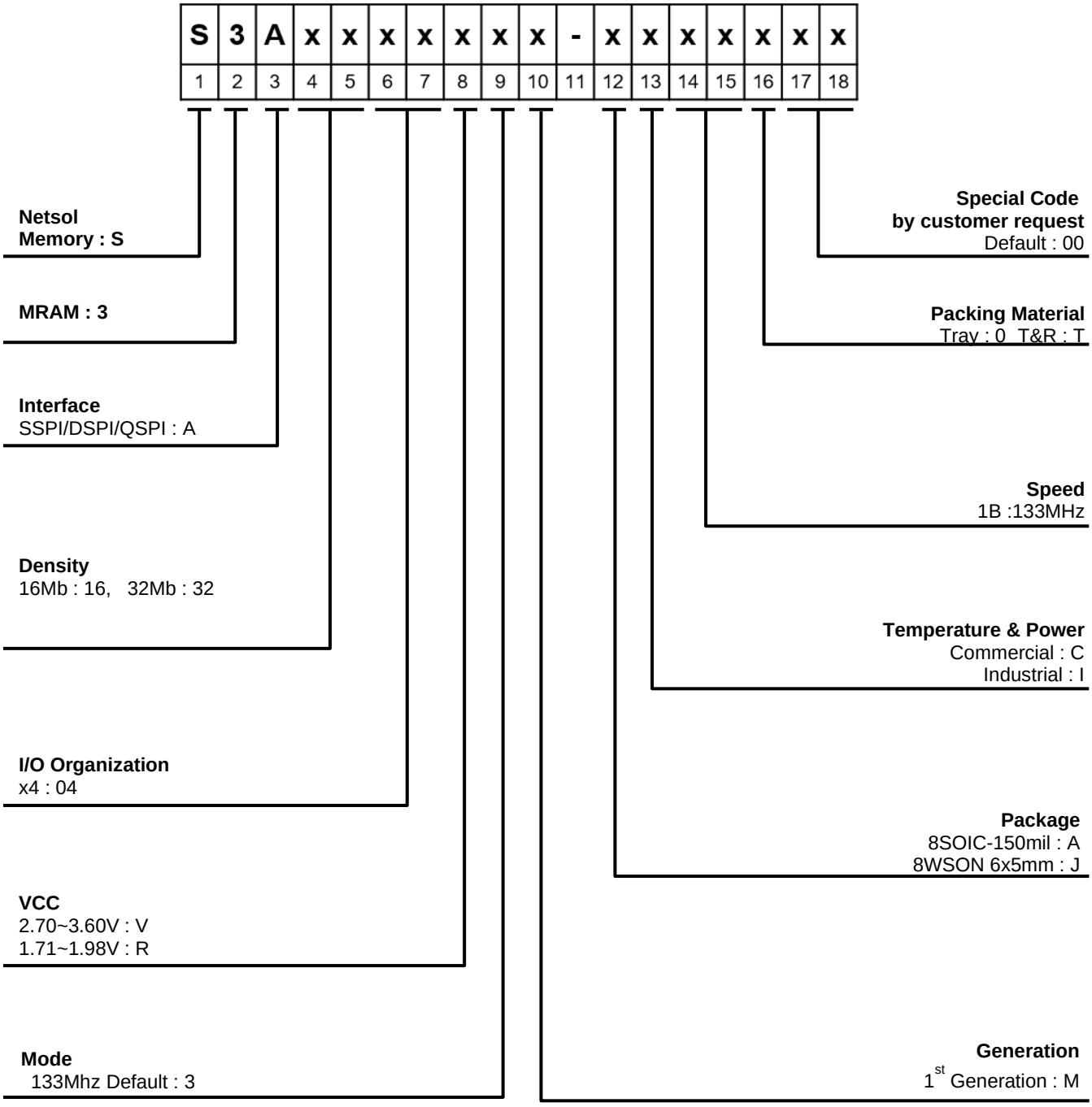


- Instruction 4-4-4 ; DRFW

Figure 70 : Timing Description of 4-4-4 DDR Instruction Type (Write with XIP)



Part Numbering System



Ordering Part Numbers

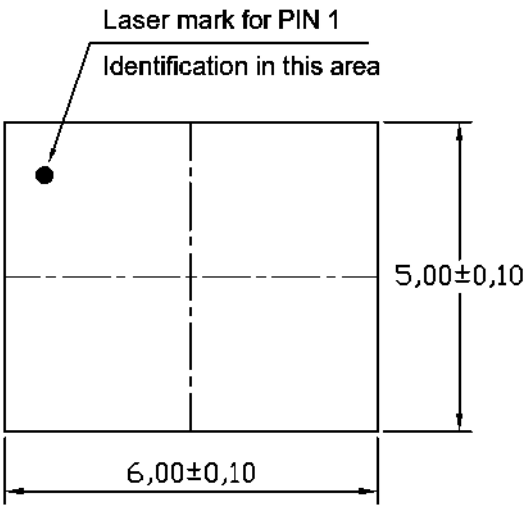
Table 38 : Ordering Part Numbers

Temperature Grade	Operating Temperature	Package	Shipping Container	Ordering Part Number
Industrial	-40° to 85°	8pad WSON	Tray	S3A3204R3M-JI1B000
			Tape and Reel	S3A3204R3M-JI1BT00
		8pin SOIC	Tape and Reel	S3A3204R3M-AI1BT00

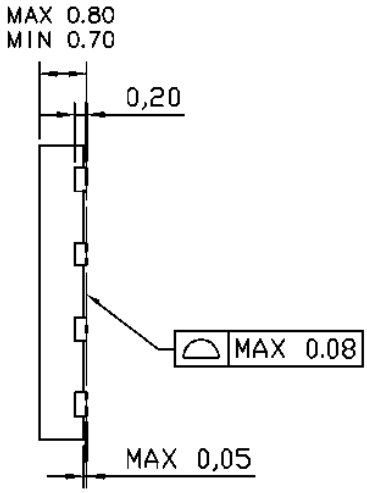
Package Dimension

8-contact WSON 6x5mm

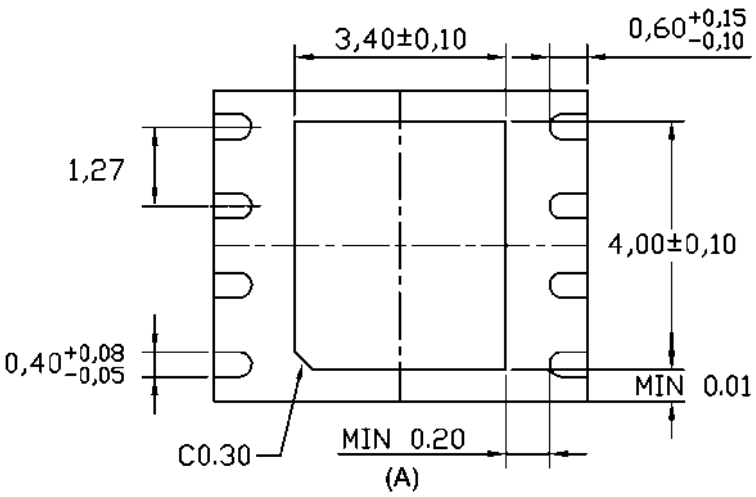
TOP VIEW



SIDE VIEW



BOTTOM VIEW

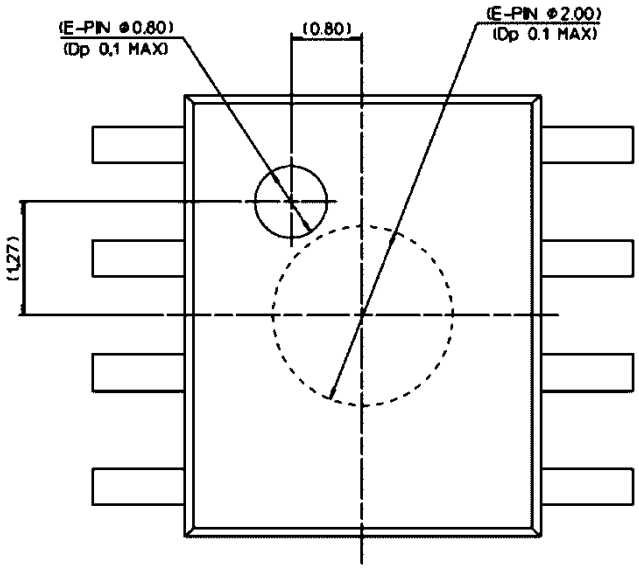


[Notes]

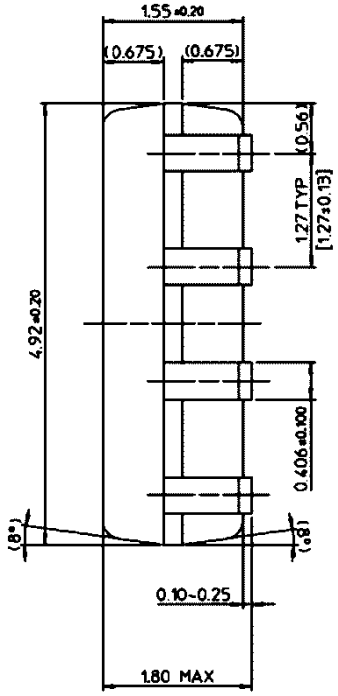
1. All Dimensions in Millimeters
2. These dimensions do not include MOLD protrusion.
3. The exposed pad size must not violate the minimum metal separation requirement (A)

8-pin SOIC – 150mil

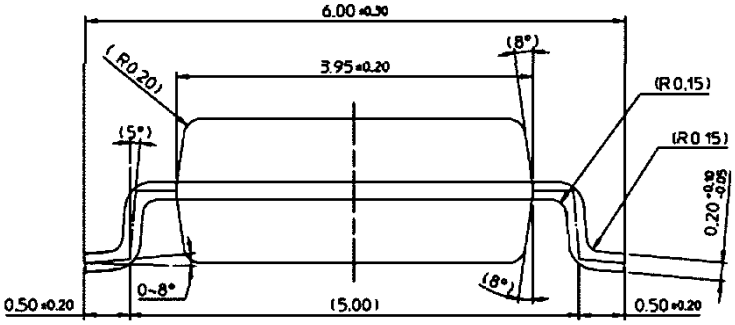
TOP VIEW



SIDE VIEW #1



SIDE VIEW #2



TITLE	8-SOP-225 PACKAGE OUTLINE	
UNIT	TOLERANCE	SCALE
mm	±0.10	N/A

Revision History

Revision	Date	Description
0.0	Jan. 2024	Initial Release
1.0	Jan. 2025	1. Update Table 9 and 10 (Read/Write Memory Array Instruction Set) 2. RDSR(05h) instruction is applicable during t_{CSDWX}.(page 35) 3. Update the Data Retention parameter (Table 29)

* Products and specifications discussed herein are subject to change by Netsol without notice.