



Application Note

64Mb Quad SPI MRAM

- **S3A6404V6M**
- **S3A6404R6M**

Single/Dual/Quad IO SPI MRAM
3.3V/1.8V

Revision 0.1

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General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM). It features a SPI bus interface, XIP(execute-in-place) functionality, and hardware/software based data protection mechanisms. SPI (Serial Peripheral Interface) is a synchronous serial communication interface with command, address and data signals.

The device consists of two 32Mb quad SPI devices, providing 4-bit I/O data access with a 2-CS#/1-CLK configuration. Each individual die can be active by its own chip select signal.

Each individual die provides various SPI modes, allowing options for bandwidth expansion. Extended SPI mode has a single pin for the command signal for each die. The user can select an option for how many pins to be allocated for address, and data signals among 1 pin, 2 pins or 4 pins. Dual SPI mode provides 2 pins for command, address and data signals. Quad SPI mode provides 4 pins for command, address and data signals.

Each individual die has its own nonvolatile register bits – status register, configuration register, serial number register, augmented 512-byte register, protection register for augmented bytes, device ID, and unique ID. The status register and configuration register are required to be set at least once on power-up after the high temperature solder-reflow process for each individual die.

This single-chip solution, featuring two 32Mb quad SPI MRAMs, ensures a minimal footprint and superior design flexibility. This device can replace Flash, FRAM or (nv)SRAM with same functionality and non-volatility.

Table 1 : Part Number

Density	3.3V Product	1.8V Product
64Mb	S3A6404V6M	S3A6404R6M

Solder Reflow

Netsol recommends the solder reflow condition as follows :

1. The peak temperature must not exceed 260 °C.
2. The time above 255 °C must not exceed 30 seconds.
3. The reflow cycles must not exceed 3 times.

Table 2 : Solder Reflow Condition

Solder Reflow Process	Max.	Units
Reflow profiles	JEDEC J-STD-020 reflow profiles	
Peak Temperature	260°C	°C
Time above 255°C	30	seconds
Reflow cycles	3	times

Multi-Die Operation

1. Chip Select Operation

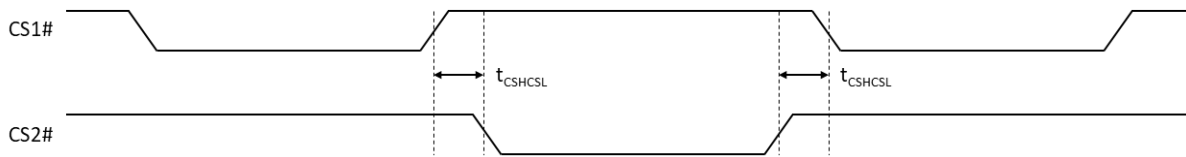
In all read and write operations for memory and augmented 512-byte area, both CS1# and CS2# are not allowed to be active Low simultaneously.

However, for Control instructions and Write Register instructions, they can be allowed to be active low simultaneously to input the same instructions or write the same data to registers.

Control Instructions	
No operation	00h
Write Enable	06h
Write Disable	04h
Enable Quad SPI	38h
Enable Dual SPI	37h
Enable Extended SPI	FFh
Enter Deep Power Down	B9h
Exit Deep Power Down	ABh
Software Reset Enable	66h
Software Reset	99h

Write Register Instructions	
Write Status Register	01h
Write Configuration Registers 1-4	87h
Write Serial Number Register	C2h
Write Augmented 512-byte Protection Register	1Ah
Write Any Register - Address Based	71h

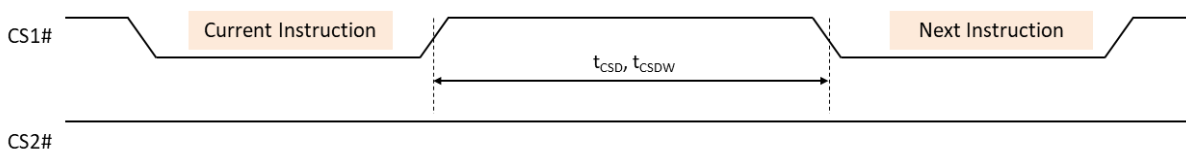
The time minimum interval time (t_{CSHCSL}) between CS1# (or CS2#) going High and CS2# (orCS1#) going Low is 0ns.



2. Multi-Die Memory Operation

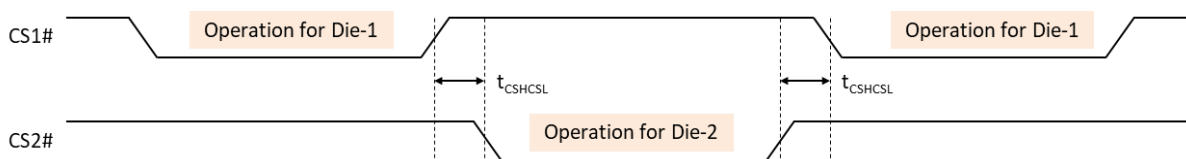
CS# High time is defined only for consecutive instructions within the same die.

(Refer to Sections the 8.7.4 and 8.7.5 of the Datasheet for detailed AC Timing Parameters.)



However, the time minimum interval time (t_{CSHCSL}) between CS1# (or CS2#) going High and CS2# (orCS1#) going Low is 0ns.

Therefore, the device can be **operated with no restriction for t_{CSD} or t_{CSDW} during die-interleaving operation.**



Initialization for Nonvolatile Register

The device has nonvolatile register bits – status register, configuration register, serial number register, augmented 512-byte area and protection register for augmented 512-byte area.

The register bits of each 32Mb SPI MRAM can be configured simultaneously only when identical instructions or data are issued to each register. However, if the register values for the two 32Mb SPI MRAMs differ, the following sequence must be performed separately for each die. ***These register bits are required to be set at least once on power-up after high temperature solder reflow process.***

Netsol recommends the following sequence.

1. power-on
 - SSPI mode is enabled after power-on, software reset or JEDEC reset.
 - Please refer to the power-on sequence in the datasheet.
2. Write the configuration registers
 - WP# =H, WREN(06h) + WRCX[87h + 4 bytes data: CR1(00h), CR2(0xh), CR3(xxh), CR4(xxh)]
 - Users can set CR1, CR2, CR3 and CR4 to the values to be used.
 - CR1(00h) makes SR[5:2] and augmented 512-byte area protection register writable.
3. Write the status register
 - WP# =H, WREN(06h) + WRSR[01h + 1 byte data: SR(00h)]
4. Write the augmented 512-byte area protection register
 - WP# =H, WREN(06h) + WRAP[1Ah + 1 byte data: 00h]
5. Users can check the register values using read register instructions.

Table 3 : Status Register-Data Protection

Bits	Name	Read/Write	Initialization State	Description
SR[7]	WPEN	R/W	0	Hardware Based WP# Protect Bit 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	SNPEN	R/W	0	Serial Number Protect Bit 1: Serial Number Write protected 0: Serial Number Writable
SR[5]	TB	R/W	0	Top/Bottom Memory Array Protect Selection 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BP[2]	R/W	0	Block Protection Bits
SR[3]	BP[1]	R/W	0	
SR[2]	BP[0]	R/W	0	
SR[1]	WREN	R	0	Write Protection Enable 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	R	-	Reserved for future use

Note : SR[7:2] are nonvolatile bits.

Table 4 : Augmented 512-Byte Area Protection Register

Bits	Name	Address Range	Read/Write	Default State	Description
ASP[7]	ASPS[7]	0001C0h – 0001FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	000180h – 0001BFh	R/W	0	
ASP[5]	ASPS[5]	000140h – 00017Fh	R/W	0	
ASP[4]	ASPS[4]	000100h – 00013Fh	R/W	0	
ASP[3]	ASPS[3]	0000C0h – 0000FFh	R/W	0	
ASP[2]	ASPS[2]	000080h – 0000BFh	R/W	0	
ASP[1]	ASPS[1]	000040h – 00007Fh	R/W	0	
ASP[0]	ASPS[0]	000000h – 00003Fh	R/W	0	

Note : ASP[7:0] are nonvolatile bits.

Table 5 : Configuration Register 1

Bits	Name	Read/Write	Initialization State	Selection Options
CR1[7]	RSVD	R/W	0	Reserved for future use
CR1[6]	RSVD		0	Reserved for future use
CR1[5]	RSVD		0	Reserved for future use
CR1[4]	RSVD		0	Reserved for future use
CR1[3]	RSVD		0	Reserved for future use
CR1[2]	MAPLK		0	Status Register TB, BP[2:0] Protect 1: Lock TB and BP[2:0] 0: Unlock TB and BP[2:0]
CR1[1]	RSVD		0	Reserved for future use
CR1[0]	ASPLK		0	Augmented 512-Byte Area Data Protection 1: Write Protection for Augmented Area Data regardless of ASP[7:0] 0: Write Protection for Augmented Area Data depending on ASP[7:0]

Note : CR1[7:0] are nonvolatile bits.

Table 6 : Configuration Register 2

Bits	Name	Read/Write	Initialization State	Description
CR2[7]	RSVD	R/W	0	Reserved for future use
CR2[6]	QPIEN	R	0	Quad SPI (QPI 4-4-4) Interface Mode 1: Quad SPI (QPI 4-4-4) Enabled 0: Quad SPI (QPI 4-4-4) Disabled
CR2[5]	RSVD	R/W	0	It must be written as 0
CR2[4]	DPIEN	R	0	Dual SPI (DPI 2-2-2) Interface Mode 1: Dual SPI (DPI 2-2-2) Enabled 0: Dual SPI (DPI 2-2-2) Disabled
CR2[3]	RL[3]	R/W	User selection	Read Latency Selection Bits : CR2[3:0] 0000: 0 Cycle 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	RL[2]	R/W	User selection	
CR2[1]	RL[1]	R/W	User selection	
CR2[0]	RL[0]	R/W	User selection	

Notes :

1. Read Latency is frequency dependent.
2. Read(03h) does not depend on Read latency Selection Bits, CR2[3:0].
3. CR2[7,5,3:0] are nonvolatile bits.
4. Extended SPI is enabled when both CR2[6] and CR2[4] are '0'.

Table 7 : Configuration Register 3

Bits	Name	Read/Write	Initialization State	Description
CR3[7]	DRV[2]	R/W	User selection	Output Driver Strength Selection DRV[2:0] 3.3V 1.8V 000: 36Ω 35Ω 001: 100Ω 95Ω 010: 75Ω 63Ω 011: 60Ω 50Ω 100: 48Ω 40Ω 101: 41Ω 30Ω 110: 29Ω 26Ω 111: 24Ω 22Ω
CR3[6]	DRV[1]		User selection	
CR3[5]	DRV[0]		User selection	
CR3[4]	WRPEN		User selection	Read WRAP Enable 1: Read Wrap Enabled 0: Read Wrap Disabled
CR3[3]	RSVD		0	Reserved for future use
CR3[2]	WRPL[2]		User selection	Wrap length configuration WRPL[2:0] 000: 16-byte wrap 001: 32-byte wrap 010: 64-byte wrap 011: 128-byte wrap 100: 256-byte wrap 101: 512-byte wrap 110: 1K-byte wrap 111: Reserved
CR3[1]	WRPL[1]		User selection	
CR3[0]	WRPL[0]		User selection	

Notes :

1. Default output strength is DRV[2:0]=000.
2. CR4[7:0] are nonvolatile bits.

Table 8 : Configuration Register 4

Bits	Name	Read/Write	Initialization State	Selection Options
CR4[7]	RSVD	R/W	0	Reserved for future use
CR4[6]	RSVD		0	Reserved for future use
CR4[5]	RSVD		0	Reserved for future use
CR4[4]	RSVD		0	Reserved for future use
CR4[3]	RSVD		0	Reserved for future use
CR4[2]	RSVD		0	Reserved for future use
CR4[1]	WRENS[1]		User selection	00: Normal: WREN is prerequisite to all Memory Array and Augmented 512-byte Area Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array and Augmented 512-byte Area Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write or Augmented 512-byte Area instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset after CS# goes High) 11: Reserved
CR4[0]	WRENS[0]		User selection	

Notes :

1. Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write instructions require WREN to be set, and WREN is reset when CS# goes high after the write instruction.
CR4[1:0] only affects the writing for memory and augmented area.
2. CR4[7:0] are nonvolatile bits.

Revision History

Revision	Data	Description
0.1	Mar., 2026	Initial Release

* Products and specifications discussed herein are subject to change by Netsol without notice.